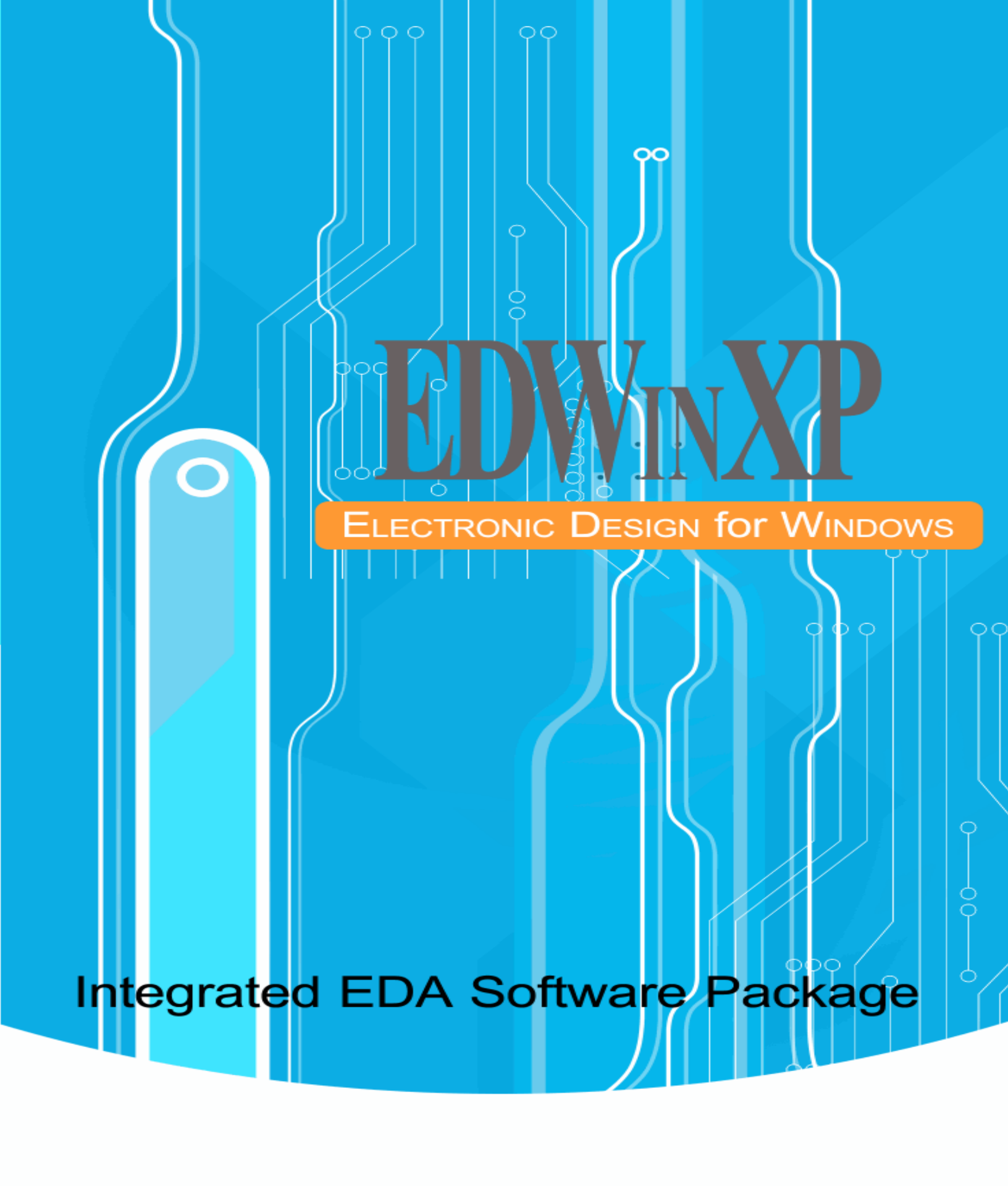
EDWinXP
Electronic Design for Windows
Integrated EDA Software Package

ELECTRONIC DESIGN FOR WINDOWS

EDWinXP

MANUAL

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Chapter 1

Introduction

EDWinXP is an EDA software package for automated design of electronic products. This integrated tool covers all stages of electronic design process -schematic capture, simulation, PCB layout design, generation of PCB manufacturing and testing documentation.

EDWinXP is a fully integrated package. Circuit designs can be front and back annotated i.e. a design may be started either from Schematic Editor or PCB Layout and design information is automatically updated. All parts of the designed project are simultaneously accessible by task-oriented modules of the system.

These task oriented modules (see Fig.1.1) are Schematics Editor, PCB Layout Editor, Fabrication Manager, Library Editor, Simulators and Board Analyzers.

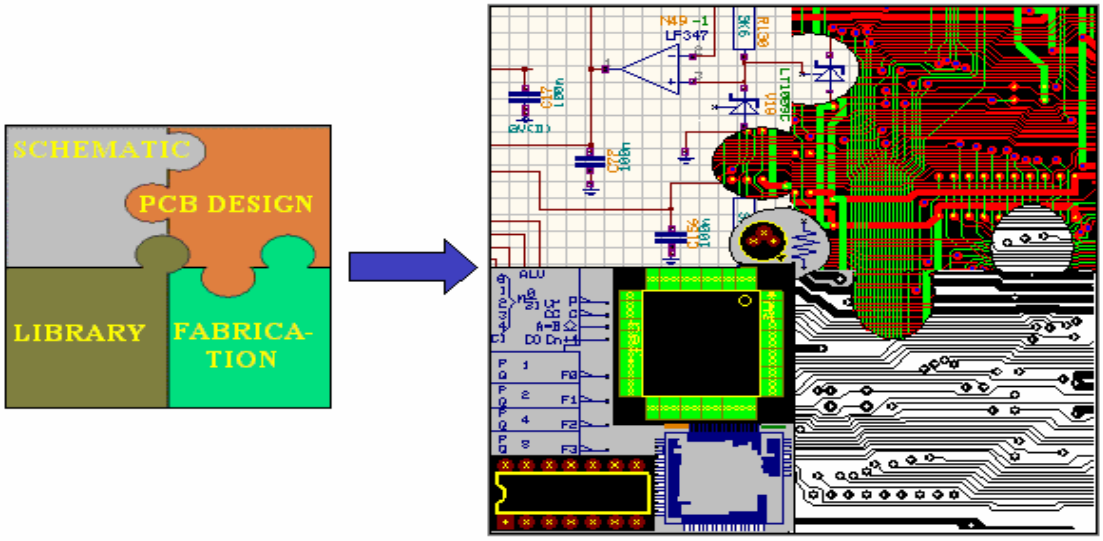


Fig: 1.1 Integrated Modules of EDWinXP

Schematics Editor: Schematic Editor captures the circuit in the form of a schematic diagram. The Schematic Diagram Editor contains a full set of manual and automated tools for placement of circuit elements on the diagram and for routing the connection. Design rules may also set for auto placement and interactive auto routing. Automatic component packaging feature generates pin-out texts on the diagram and prepare the circuit for PCB layout design. Circuits defined in VHDL or in SPICE format netlists may be also imported and converted into schematic diagrams. Due to the integrated structure of EDWin, subsequent design changes in real-time are front annotated to the PCB layout.

PCB Layout Editor: PCB Layout editor includes full set of manual and automated function for designing 32 layered boards. Dedicated full board auto router module is

integrated with PCB Layout Editor. Design rules for manual, semi-automatic and automatic routing of traces and component placement can be defined and may be set individually for each project. There are provisions to check design rules violation, clearance errors and missing or incomplete connections of the circuits in this module.

Fabrication Manager: CAM tools grouped in this module allow generating all necessary documents for manufacturing, testing and assembly of printed circuit boards. Fabrication manger also includes reverse engineering tools for reconstructing circuit designs from available manufacturing data in graphical form (artworks in Gerber formats, DXF format drawings etc). RS-274D and RS-274X are supported by EDWin. Gerber ASCII file viewer, an integral part of this module enables to verify artworks before sending them for plotting and manufacturing.

Library Editor: EDWinXP component libraries may be updated, customized or enhanced with the help of Library Editor. Functionality of this module allows definition of graphical representation of components in schematic diagram (Symbol Editor) and on Printed Circuit Board (Package Editor). These elements are included then in the component description, which also contains the packaging information, thermal parameters and link to simulation modules. 2D and 3D views of component packages are created according to IPC, JEDEC and EIA standards.

Simulators: Simulator supports various analyses of digital, analog and mixed circuits. It allows testing of the circuits without having to build them thereby reducing the development time and cost on a wide parameter range easily. EDWinXP provides two types of simulators one is Mixed Mode Simulator, the system's native circuit level analyzer and other is EDSpice Simulator, the full implementation of XSPICE as defined by Georgia Tech.

Board Analyzers: The Electromagnetic Analyzer and Thermal Analyzer checks the integrity and correctness of layout design.
Electromagnetic Analyzer presents graphically the predicted intensity of electromagnetic fields inside and outside board boundaries. The Signal Integrity Analyzers detects distortion, noise and crosstalk for critical signals.
The temperature distribution on a finished PCB may be analyzed graphically with the help of Thermal Analyzers.

Integrated Structure of EDWinXP

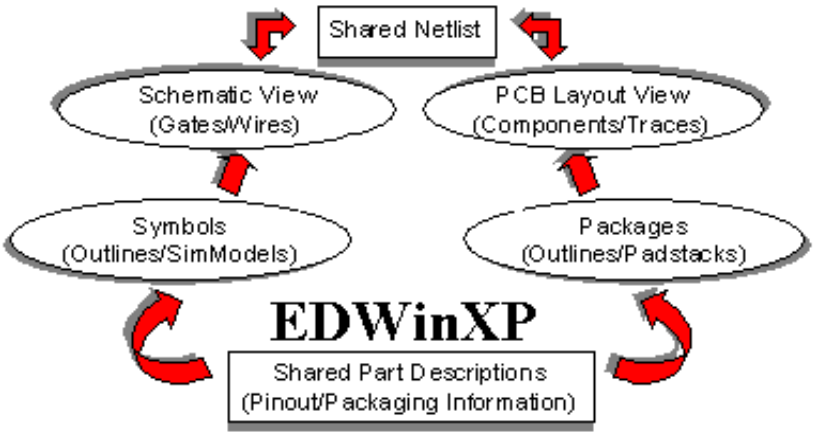


Fig1. 2 Integrated structure of EDWinXP

EDWinXP has a totally integrated structure as shown in Fig.1.2. It features seamless integration between all its modules facilitating automatic front and back annotation.

The Schematic and Layout editors make use of the libraries which have shared part descriptions. Part description contains all information about layout view (package) and schematic view (symbols, packaging and pinout) of the component.

When we refer a part, it would extract the physical component assigned at the time of part creation. Some Parts do not contain the symbol information or sometimes the package information. Those parts, containing both symbols and package, will only take part in automatic front annotation to the layout and vice versa.

Components are added to the Schematic diagram from the library and are referred to as Parts; to complete the design we have to establish the connectivity between the components. The connections are created with the support of CONNECTIONS (in Schematic) and TRACES (in Layout) or NETS (in both Schematic and Layout).

The common netlist for schematics and layout is built, through packaging. When a component is packed in schematics, the component pin will get its equivalent pinout information in layout, and are stored as node information. The net consist of nodes and each node has its reference to the components pins both in schematics and layout.

Thus when component in schematics is packed, the layout pin equivalents are retrieved from information stored in part description. Every pin of packed schematics component is checked whether it is a node in some net, if it is a node then the node info is updated. Thus the corresponding package and pinout information's are front annotated to the PCB layout editor and vice versa as shown in Fig 1.3.

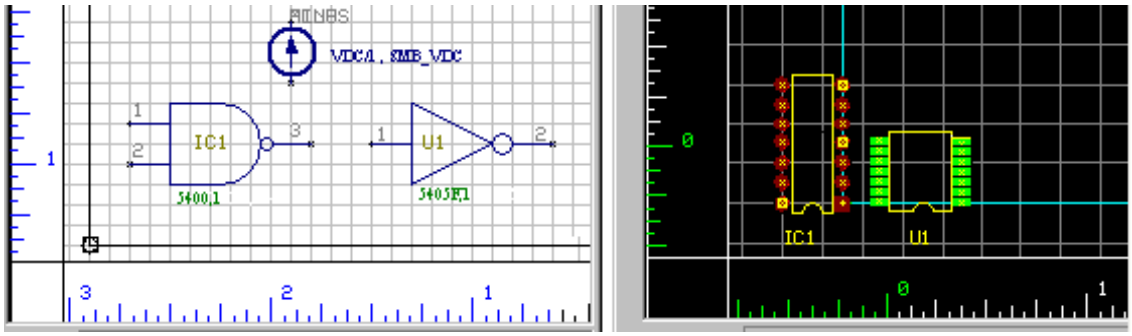


Fig1. 3 Front Annotation

Structure of Project Database

All data about electronic design which may consist of several circuits and sub-circuits is stored in a single database, along with PCB layouts. All parts of the project design - schematics, PCB layout and PCB fabrication drawings and documents are simultaneously accessible by task oriented software modules of the system.

An individual project supports circuit with multiple hierarchical levels with multiple pages within a hierarchy. All hierarchies are loaded into memory and stored on disk in a single standard project (.EPB) file. All hierarchies share the local part and

libraries. The project allows the user to create up to 99 hierarchies. Each hierarchy may consist of 1 to 99 pages of schematic diagram and a single PCB layout.

There is main hierarchy (MAINHIER) and all further hierarchical circuits that the user creates, are either under this main hierarchy or in equal priority level. The highest level contains a normal circuit, with the other hierarchies being used to capture subcircuits. If required, the designs which are reused can be saved as subcircuits. The circuit can be then referenced as a single component, the subcircuit instance.

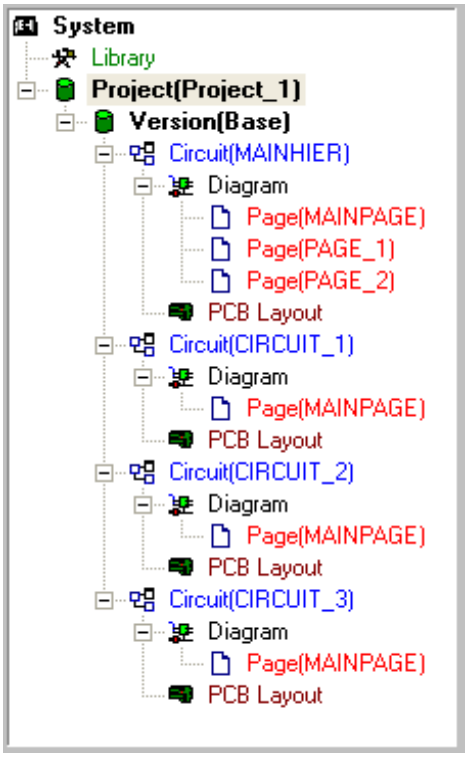


Fig: 1. 4 Hierarchies

Subcircuits can be of two types, hierarchical subcircuits and library subcircuits. Subcircuits may be nested within one another. Subcircuits allow hierarchical construction of designs by grouping the elements of a circuit into a macro. Circuits can be saved as a subcircuit in the subcircuit library and later may be adapted to a symbol.

While simulating the hierarchical subcircuit in Mixed Mode Simulator, the lower hierarchy subcircuit is flattened with upper hierarchy circuit. On other hand in EDSpice Simulator, the library subcircuits (.SBC files) are merged to the spice netlist file. And this entire circuit is simulated.

The fundamentals in designing the PCB are done in Layout Editor. Each hierarchy will have a separate Layout (PCB) associated with it. This means that the entire circuit

for a single PCB must be created on the same hierarchy. Any circuit created on any other hierarchy will be created as a separate PCB for that hierarchy.

Integrated Project Database Principles

The integrated structure of the project is explained briefly. You can start with capture of the design in the form of Schematic Diagram. The initial stage will be to place on the schematic, the components, required in the circuit. Assume that one of the components required is IC7400. All the information about this particular component is stored in Part library files.

The part library consists of 3 separate but cross-referenced libraries one each for the part descriptions (*.PART), symbols (*.SYMBOL) and packages (*.PACKAGE). The data in the part description stores the information that four gates of 7400 require a 2 input NAND symbol for graphical representation in the diagram (Schematic components), that a 14-pin DIP package is needed to represent this component on the PCB Layout. The part will also contain Pin out information, i.e. information about which pin in Schematic refers to which pin in PCB footprint. These are needed to front annotate circuit components from diagram to PCB Layout - to automatically generate Layout components

A typical example of components placed in Schematic and Layout editor is shown in Fig 1.5. When the components in the circuit are created, all necessary library elements are loaded from part libraries on disk files and appended to the Project library (local library) within the project. Each new instance of the same type of component requires only a reference to the library elements, i.e. even if there are say 15 NAND gates in the project, the Project Library will contain only one instance. This means that even if several identical components are used in the circuit - they all refer to the same set of library elements in the project (local library).

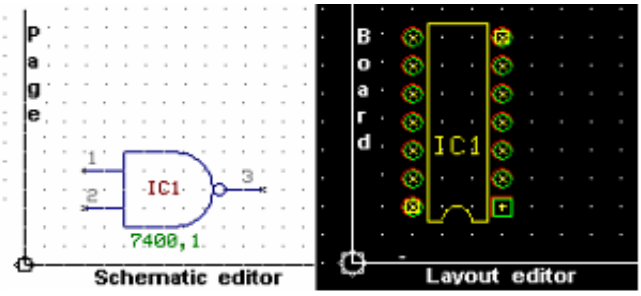


Fig 1.5 Components placed in Schematic and Layout editor

In addition to the process of creation of components and placing these components on the project (database), to complete the design we have to establish the connectivity between the components. The connections are created with the support of CONNECTIONS (in Schematic) and ROUTE (in Layout) or NETS (in both Schematic and Layout). There are 32 layers available of which 4 layers are reserved for component and solder side silk screens (COMP.PRINT and SOLD.PRINT), component and solder side solder masks (COMP.MASK and SOLD.MASK) and the rest 28 layers as trace layers.

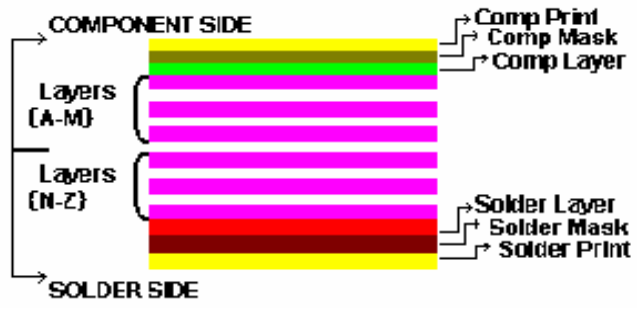


Fig: 1.6 PCB sides and layers in EDWinXP

Fig. 1.7 describes logical connections between component entries in the circuit. The net consists of one or more nodes (component entries after connection) and is connected with connections/ traces (physical representation) on Schematic/ PCB Layout. Each Connections/ Trace which may consists of one or more segments is always assigned to a net Therefore operations performed on nets and nodes may result in changes to traces and connections.

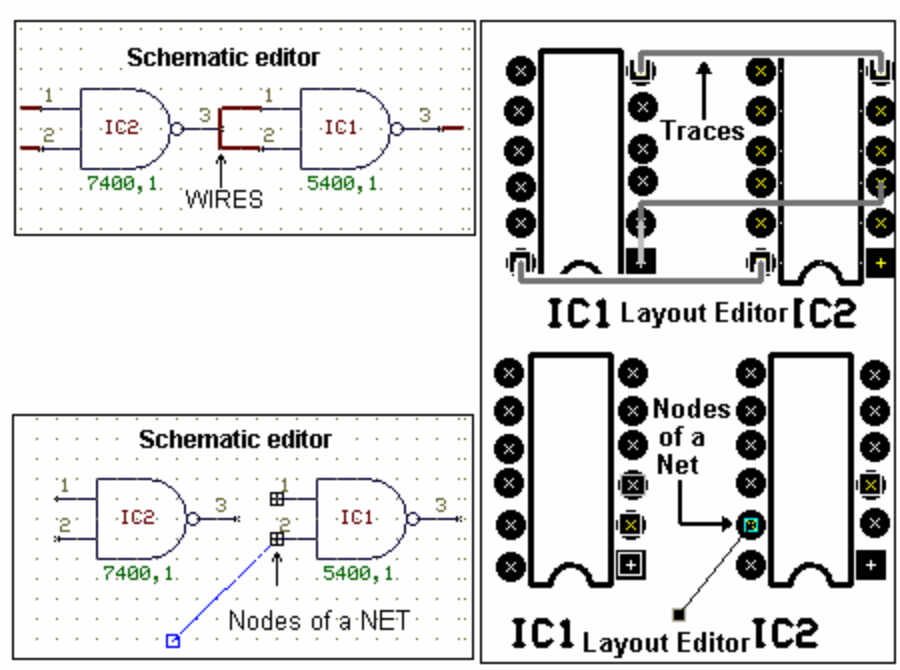


Fig1.7 Wires, Nets and Traces

In Schematic editor, connections between component entries may also be wired using BUSES. Bus is a group of wires carrying signals. These wires are called Bus Members and should be joined in branches (T-connected) by junction points. Each bus member has a specific number and assigning same bus member number creates merged nets. The net names and bus member numbers may be set under Preference/ Instant Wire label, to appear immediately in the form of movable text labels and may be placed as shown in Fig. 1.8.

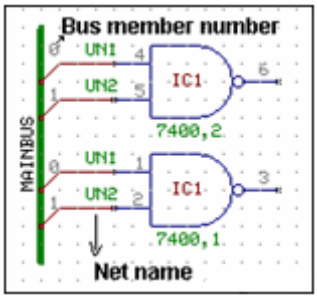


Fig1.8 Inserting text labels

In Fig: 1.8, the connection having same bus number belong to same net

Each Trace, which may consist of one or more segments, is always assigned to a net. Nets are considered fully connected if all the nodes in the net have routed connections. All traces, which connect a net, must create an uninterrupted path with branches joined together at component pads or by T-connections to vias or bending points. Trace segments may be placed on any of the trace layers. The board may be checked for errors and rectified to produce an error free board with the Connectivity check and DRC check.

The Design/Page/Board description notes usually consisting of texts and graphics may be used to complete the Schematic diagram and PCB Layout with additional information. The difference between Design and Page notes is that Design notes are common and visible on all pages of the Schematic diagram (For e.g.: Design notes may be used to form the outline of a table, name given to the project which appears on all pages) whereas Page notes are specific to the defined page (for e.g. Page Notes may be used to fill the table with texts containing information regarding the page). See Fig. 1.9 shown for the same project (database). You may notice that design note (HALF ADDER) appear in main page and in new page whereas page notes (Page1 of 2) appears in the defined page.

In the same way as Schematic, the Layout may be furnished with board description notes and dimensions, which may be used during fabrication.

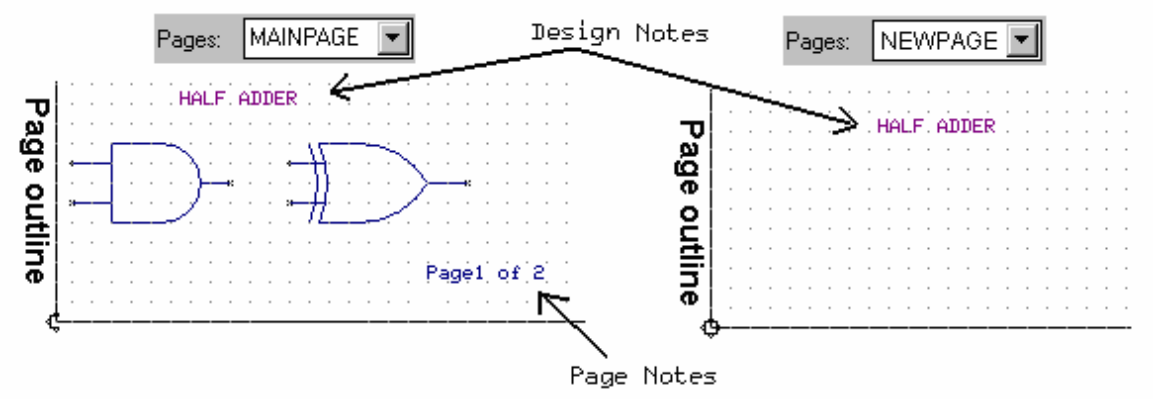


Fig1.9 Design / Page / Board description notes

You can set the dimensions in fabrication manager and enable the display of dimensions in layout editor from view /layout view /dimensions.

The final step of design process is to generate required design validation outputs and PCB manufacturing documentation. This task is handled by fabrication module.
Example for drill data and artwork generated by the fabrication module is shown in Fig. 1.10

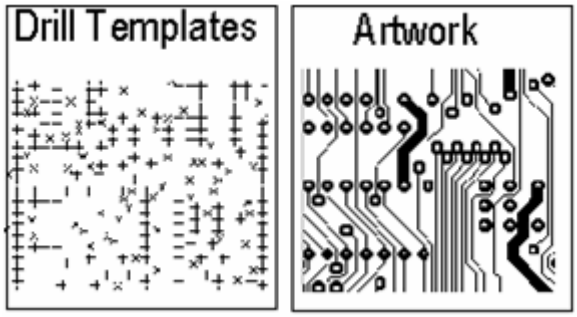


Fig1.10 Drill data and Artwork

Anytime during the work, the whole project (database) may be stored on the hard disk in a single file (extension *.EPB)

Workflow in EDWinXP

Capturing Schematic diagram of the circuit

The user may start to create the integrated design project (database) by either capturing the circuit in the form of a diagram or by designing its PCB Layout. This concept allows building both parts of the circuit design simultaneously. However, the most practical way to design a PCB is to capture the circuit by creating its Schematic diagram first.

Simulation of the circuits (Optional)

After completing the Schematic diagram, simulation may be performed on the circuit. It is a process of replacing the circuit symbols with their respective models and analyzing the circuit's behavior under different conditions. Two types of circuit analysis may be performed. You can simulate circuits depending on the availability of simulation models for components present in the circuit.

- Mixed mode Simulator is integrated into the system for circuit analysis. The Simulator also contains a Waveform Viewer, which is a graphical presentation tool used to display the results of the simulation.
- EDSpice Simulator is a separate plug in. It provides the facility to analyze and validate the functionality and behavior of circuits captured in the form of Schematic diagrams. The EDSpice Simulator is based on SPICE 3F5 and XSPICE

  with a number of extensions and improvements. Different types of analysis may be performed and the result may be obtained in Printer, Plotter also in Waveform Viewer.

 *Both the above simulators can simulate analog, digital and mixed circuits*

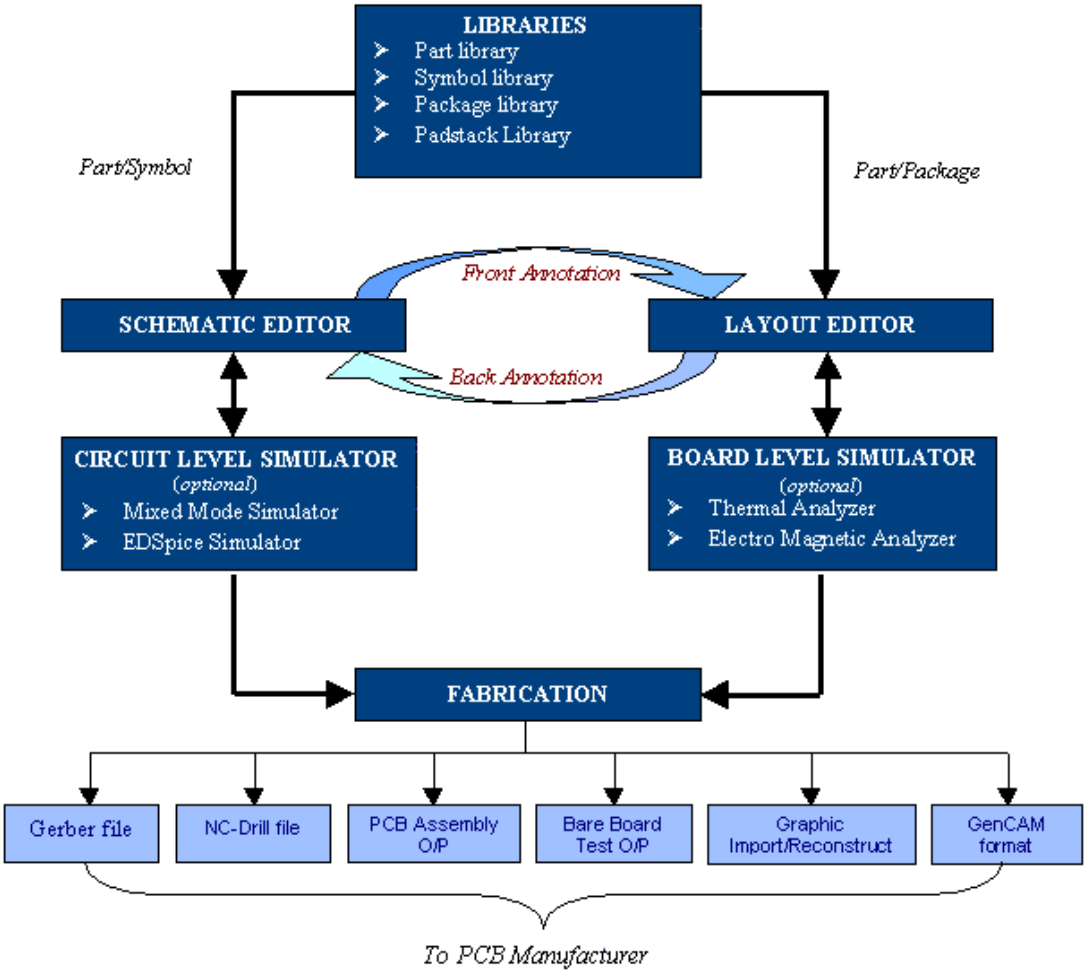


Fig1.11 Work flow in EDWinXP

Design printed circuit layout

If the circuit has been captured in the form of Schematic diagram, the next step would be to design the PCB. Due to the integrated project concept, the components placed on the Schematic and the netlist information will be front annotated to the Layout. Here the important aspects of this module are automatic placing of components, automatic clearance & connectivity check and autorouting.

Without using Schematic Editor, the PCB design may be started directly from the Layout. Thus all changes concerning netlist and circuit components introduced during PCB Layout editor process will be automatically updated in the Schematic Diagram (Back annotation).

Analyzing the Board

Different types of analysis may be performed on designed PCB to find out how component placement and the way the connection are routed may influence the functioning of the circuit. There are two types of analyzers.

- **Thermal Analyzer:** To calculate and present thermal effects generated by component on the board.

- **Electromagnetic Analyzer:** To predict the intensity of magnetic field generated by the working circuit on the PCB. This analyzer includes also Signal Integrity Simulation.

PCB manufacturing and testing documentations

Usually the fabrication of the Layout is the final step of circuit design. This part consists of several tasks resulting in completing the PCB manufacturing documentation. The tasks include optional creation of copper areas, adding dimensions and notes, printing Layout documentation drawings, extracting NC-drill data to disk files or paper tape, editing, dimensioning and printing of drill templates, editing and printing of layer artworks, generation of artwork data files in Gerber ASCII format, preview of artworks in Gerber ASCII files, generation of disk files containing generic data for Pick & Place machines. Special PCB fabrication aid items may also be placed.

The Graphic Import Editor allows importing / reconstructing (Reverse Engineering Process) PCB from the Gerber files. This combined with its unique ability to import Schematic netlists makes this to be a helpful resource for OEMs and PCB learning systems (REVENG – www.whingate.co.uk)

Chapter 2

EDWinXP Project Explorer

The Project Explorer provides access to all the modules of EDWinXP. Physical and logical view of EDWinXP Explorer is practical when working with hierarchy. Logical view shows the relationship between the circuit hierarchies, whereas physical view just displays the circuit hierarchy.

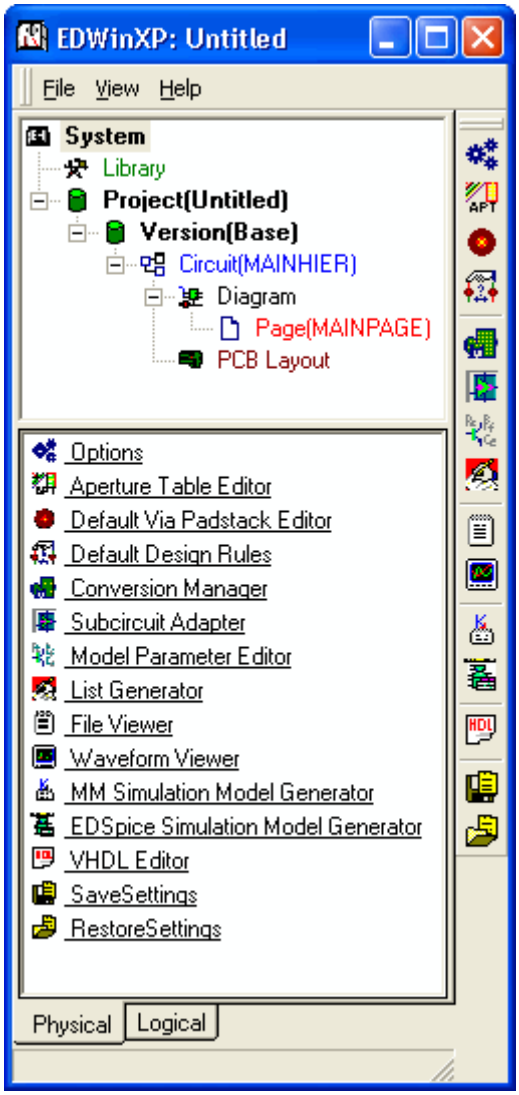


Fig: 2.1 EDWinXP Project Explorer

Briefly, the main menu consists of:

- File opening and saving of projects.
- View Enable/ disable the view of task lists and task toolbar.

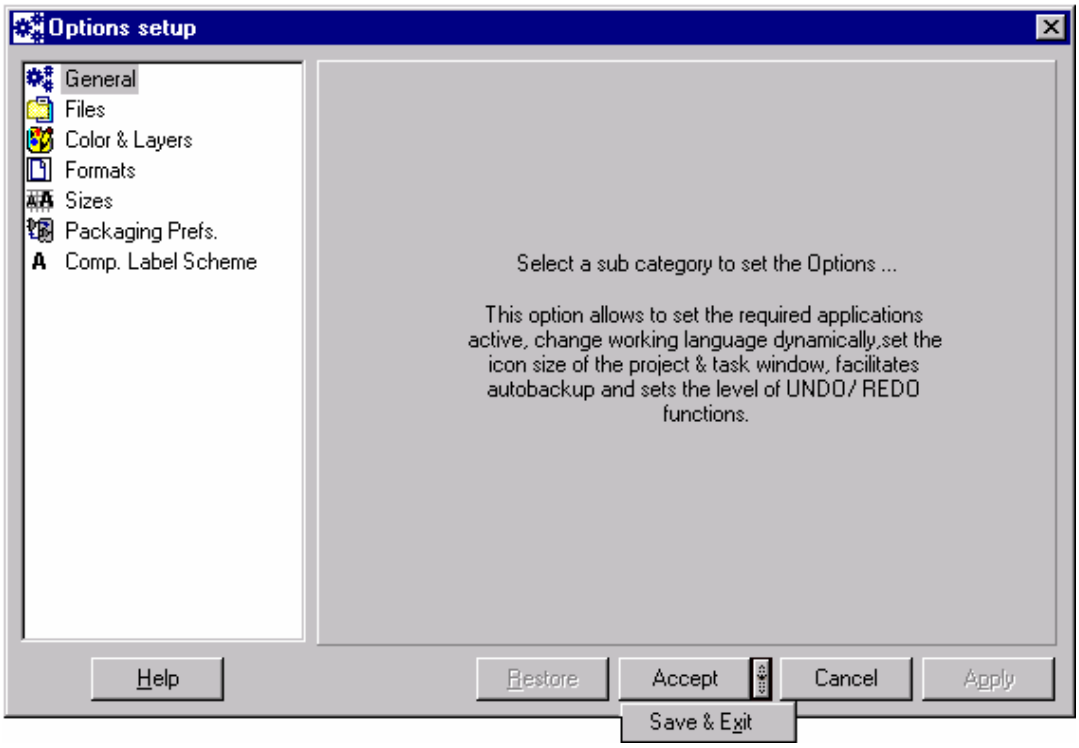
In addition to the main menu functions, there are a number of options that enable the user to work with the various modules and editors of EDWinXP. These are briefed below.

System

System Contains the default option set, file viewer, conversion manager, Sub circuit Adaptor, Model Parameter Editor, Waveform Viewer, Save, Restore settings etc.

Options

EDWinXP Options in the Tasks Window is meant for either implementing the default settings or changing the current settings and implementing it. The various options available include:-General, Files, Colors & Layers Names, Formats, Sizes, Packaging preferences, Schematic Components Labeling Scheme. The options can be invoked from *Project Explorer-> System->Options*



The settings that are changed can be viewed by clicking on the ***APPLY*** button in the Options window. These changes stay for the current project. This action is similar to clicking the ***ACCEPT*** button. To make the changes permanently, click ***SAVE & EXIT*** option by clicking the drop-down of ***ACCEPT*** button. Click ***CANCEL*** button in order to exit the window without saving the changes. ***RESTORE*** button is used to restore the default values.

General Option

The General option let you choose settings that determine:

Active Application The applications which are required in the startup of EDWinXP may be set here. The applications that may be set are Schematic editor, Layout editor, Library Explorer and Library Browser.

Language The working language may be dynamically changed using this option.

Icon Sizes The Icon size for project explorer and task list may be changed suitably.

Recovery & Units Alternative to ordinary save, you can set EDWinXP to automatically take a backup copy of the project you are working to avoid loss of work. The backup copy (*.BAK) saves the project according to the time interval set and takes the name of the project. The minimum allowed time is 1 minute.

Apart from backup facility, the UNDO/ REDO level may be set here. The level of undo/ redo operation affects the system speed. That is, increase in the number of UNDO/ REDO steps, decreases the speed.

The units may be set using this option to override the units set in individual modules.

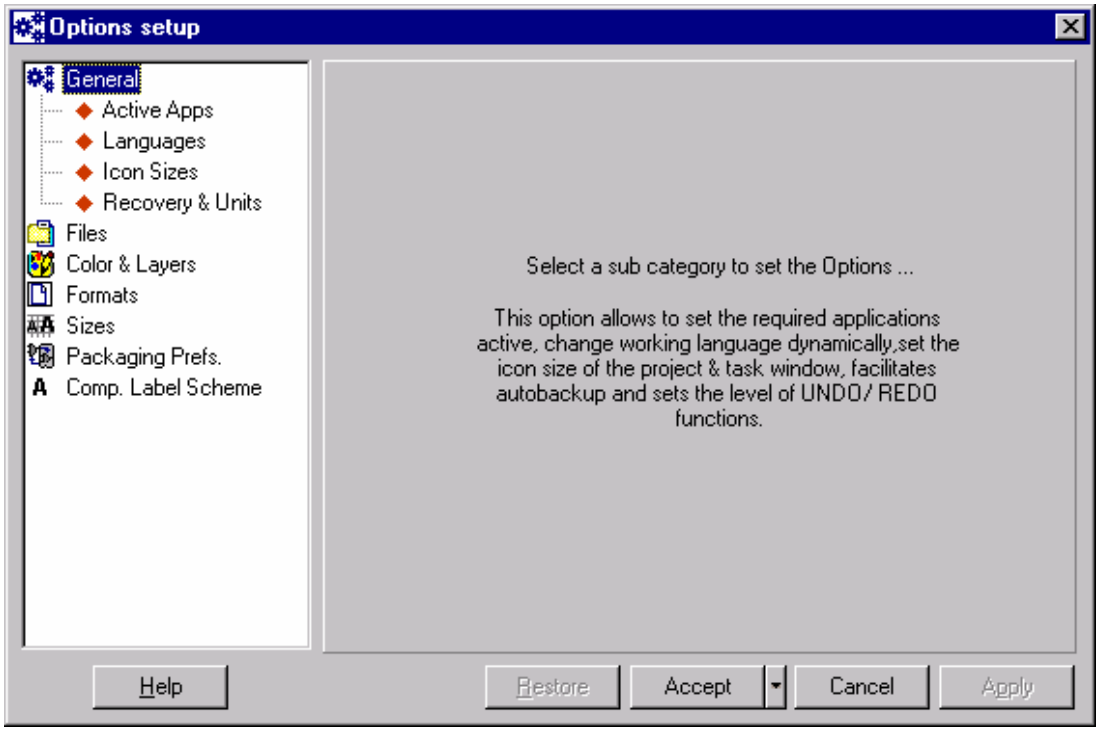


Fig: 2.3 General options

File Option

The File option let you choose the working directory for System files, Job files and EED3 files. Paths are set by default. In order to change the path, click the cell containing the path. Another window pops up from where the desired path may be

selected. Click ***OK*** to set the path and exit the window. This new path is seen in the corresponding position under the Selected Path column.

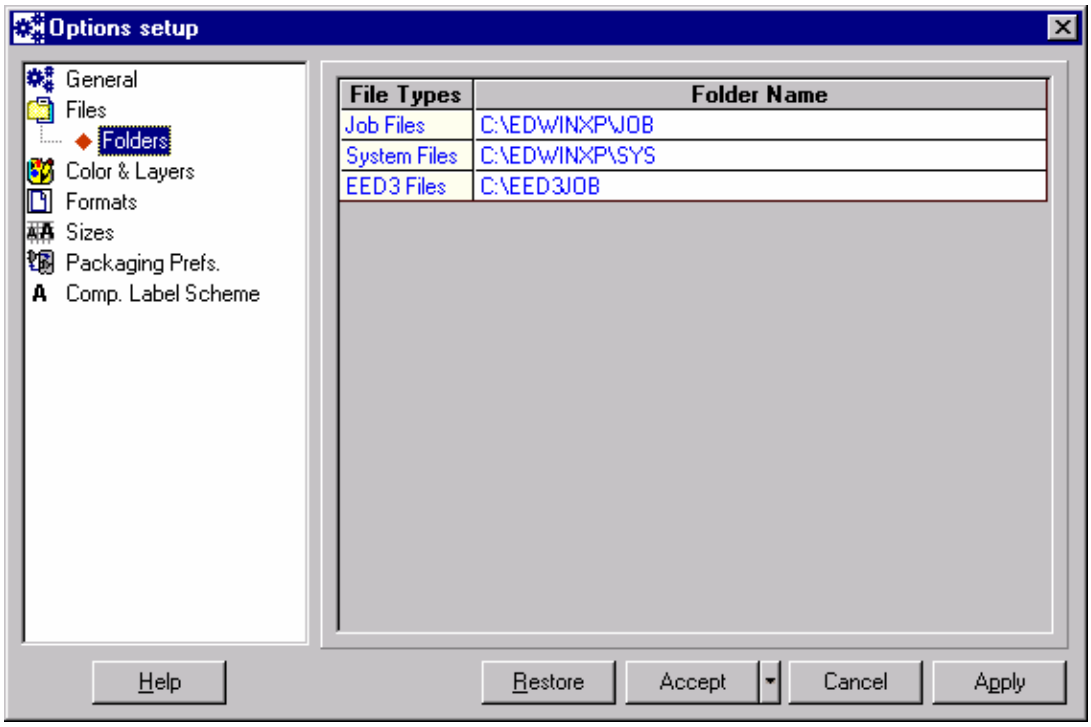


Fig: 2.4 File options

Color & Layers Option

This option when selected sets the default colors for the various items in Schematic and Layout editors. It also sets the default colors for the 32 layers of the PCB. This window consists of three sections, each of which has been explained below.

Schematic Categories

Assign colors for various schematic categories such as component outline, component name, etc. to the notes being included in the schematic diagram. On selecting this option, a default set of colors has been assigned to the various schematic categories. These may be changed by first selecting the category and then, choosing the color from the palette available.
The change gets enforced immediately in the preview part of the window as well as in the Color column. The type of grid (line, dot or cross) to view may be selected on right click.

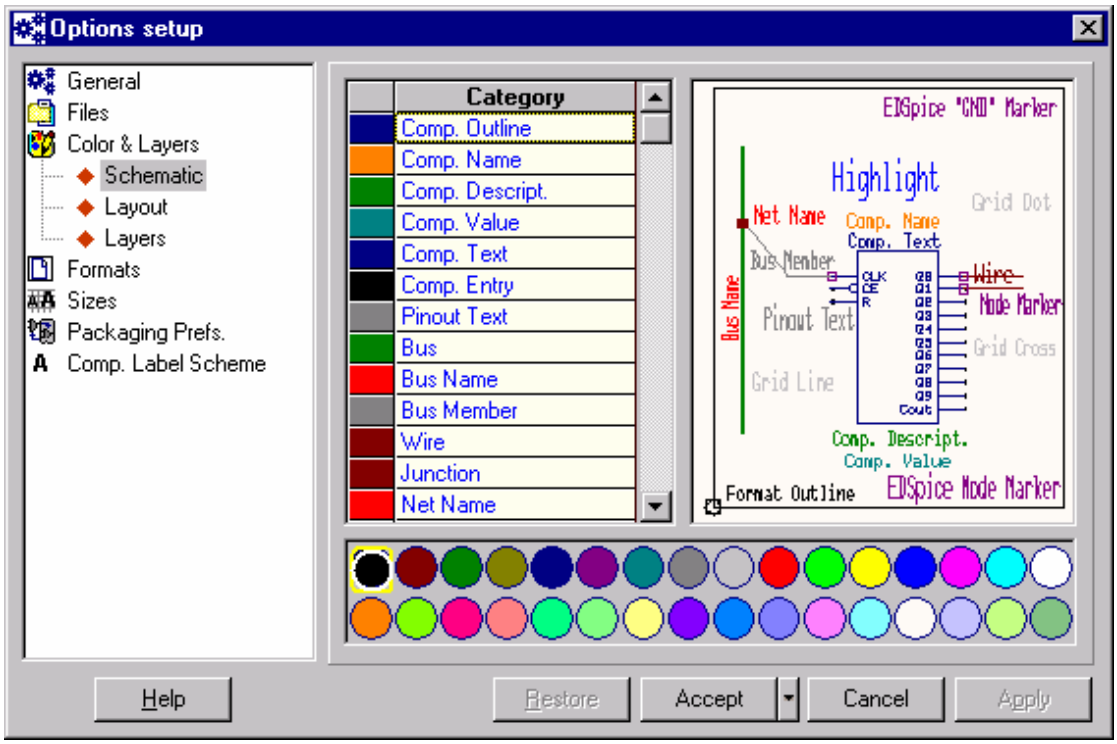


Fig: 2.5 Schematic Categories

Layout Categories

Set the coloring pattern for various categories such as grid, background etc. of the layout. On selecting this, a default set of colors has been assigned to the various layout categories. These may be changed by first selecting the category and then, choosing the color from the palette available. The change gets enforced immediately in the preview part of the window as well as in the Color column. The type of grid (line, dot or cross) to view may be selected on right click in the previous area. Also True Size may be selected on right click.

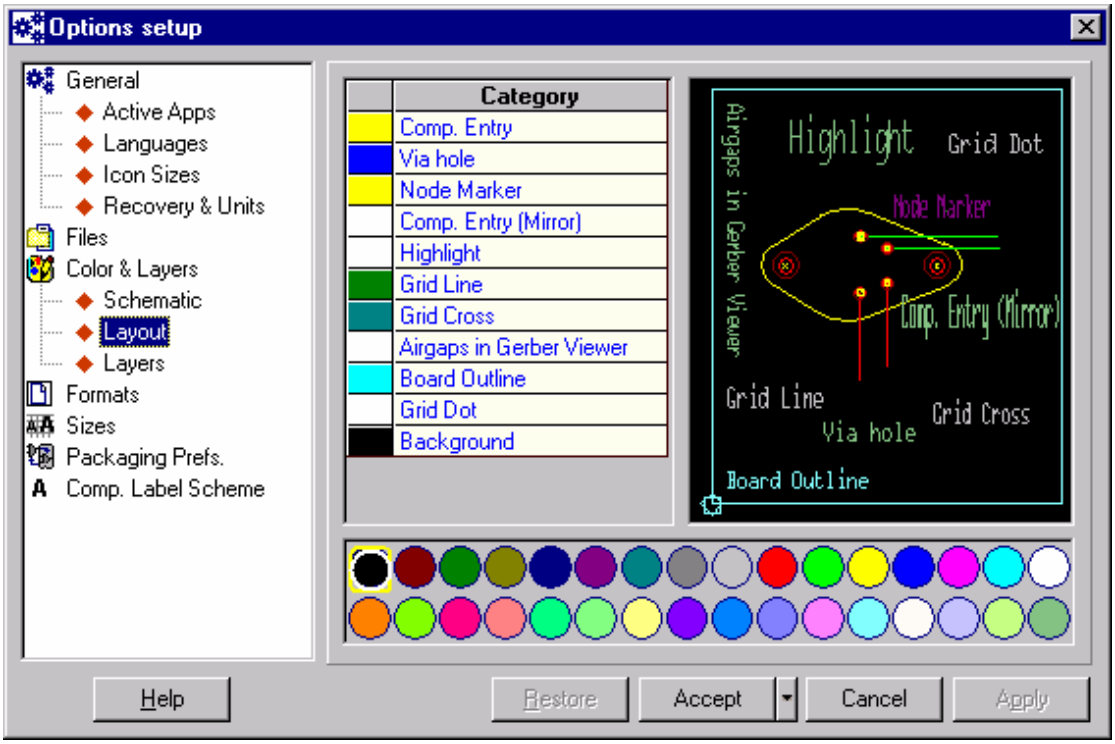


Fig: 2.6 Layout Categories

Layers

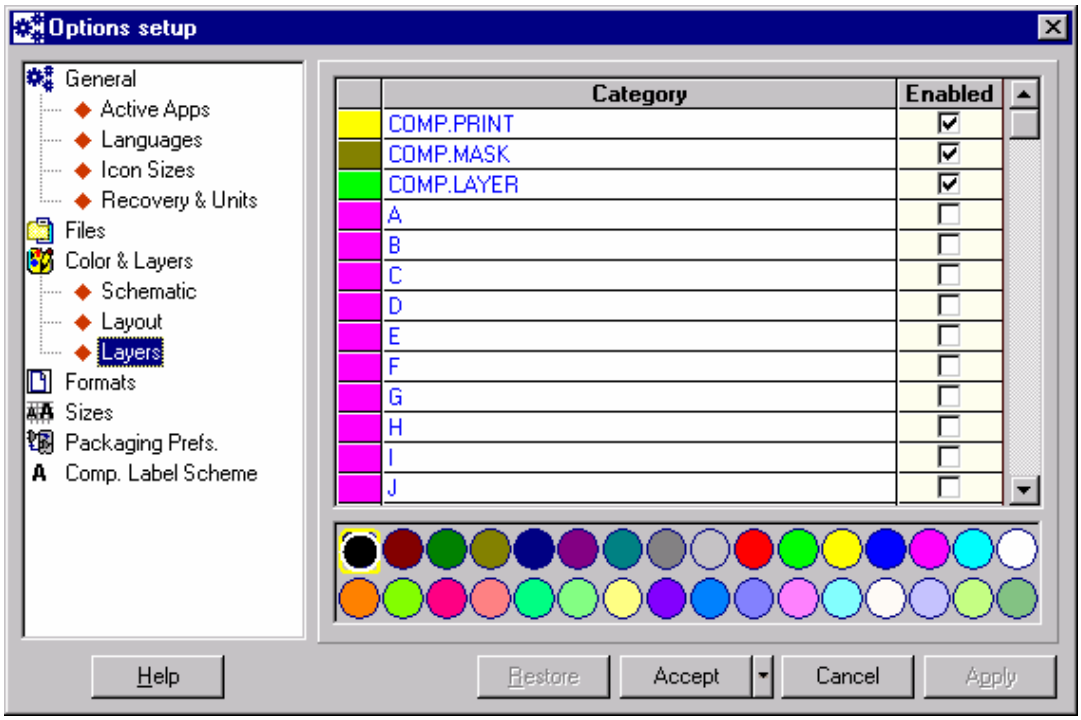


Fig: 2.7 Layers Categories

Set the default colors of 32 layers in Layout Editor. On selecting this, a default set of

colors which has been assigned to the various layout categories may be changed, by first selecting the category and then, choosing the color from the palette available. The change gets enforced immediately in the preview part of the window as well as in the Color column. The names of the layers may also be changed here.

Formats Option

The Formats option let you choose the format for the Schematic Page and Layout Board size. If no default size is selected, system assigns a random size. American and European default format sizes are also displayed.

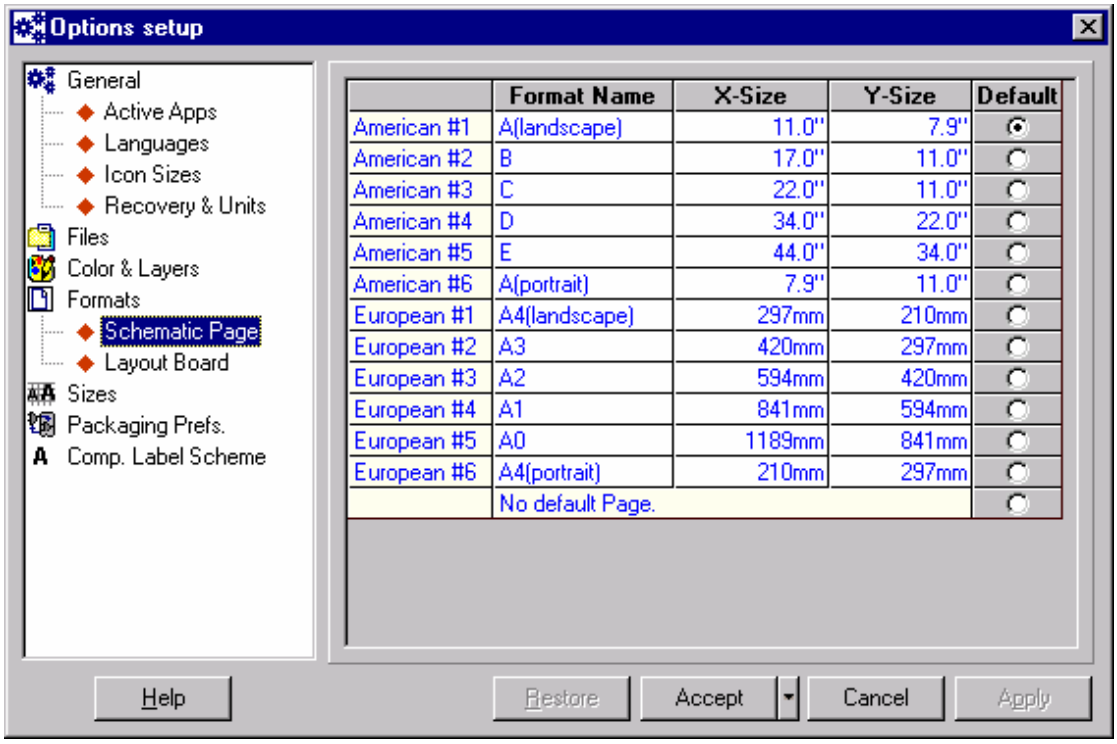


Fig: 2.8 Format option

Selecting each option displays a window with a set of default formats. These may be edited by double clicking the value to be changed. Formats for both pages format and board outline may be set in this window.

Sizes Option

This option when selected set the default sizes of various categories. Each of these options has been explained below.

General

Angle Snap: Defines the angular steps for rotation of a symbol in degrees from the existing set or by entering new values by double clicking the required row.

Pick Area: Allows setting values in pixels as the least capturing area when selecting graphic items in inches or millimeters from the given set of values. New values may be entered by double clicking the required text box.

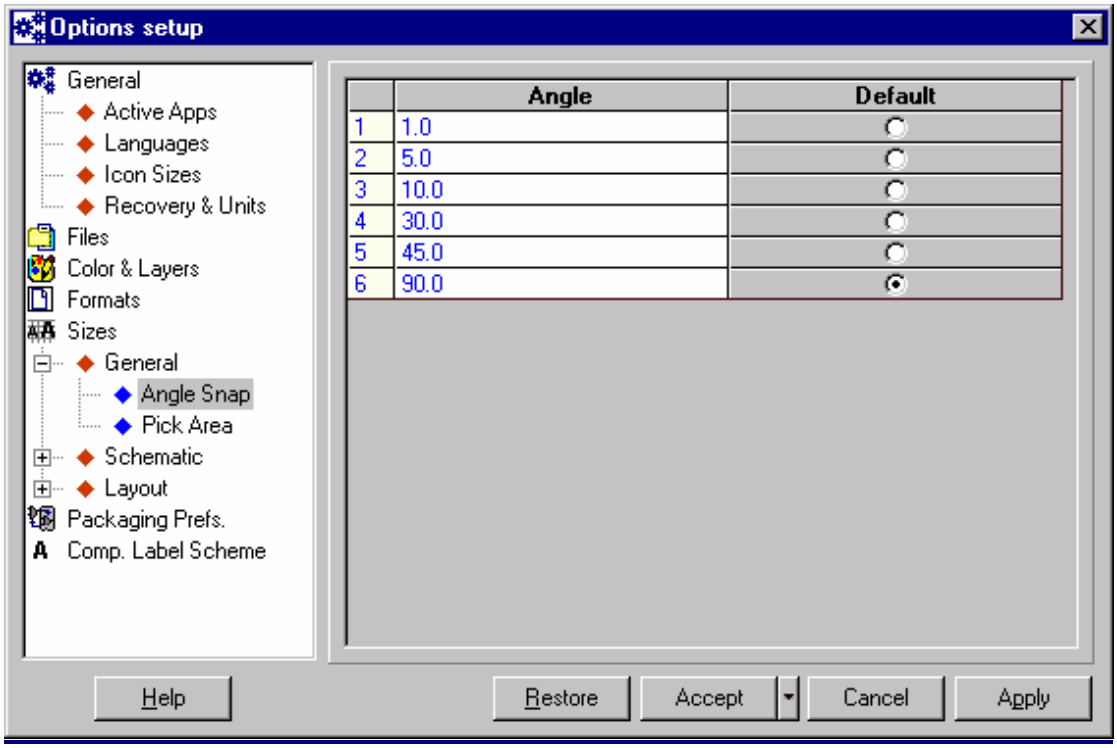


Fig: 2.9 Sizes option

Schematic

Schematic Text: This option sets the default height and line width of schematic texts. A set of default values is displayed on selecting this. These may be changed by double clicking the value to be changed. The change is visible in the Preview part of the window immediately. Given below is a brief description of the parameters provided in the Fig.2.10.

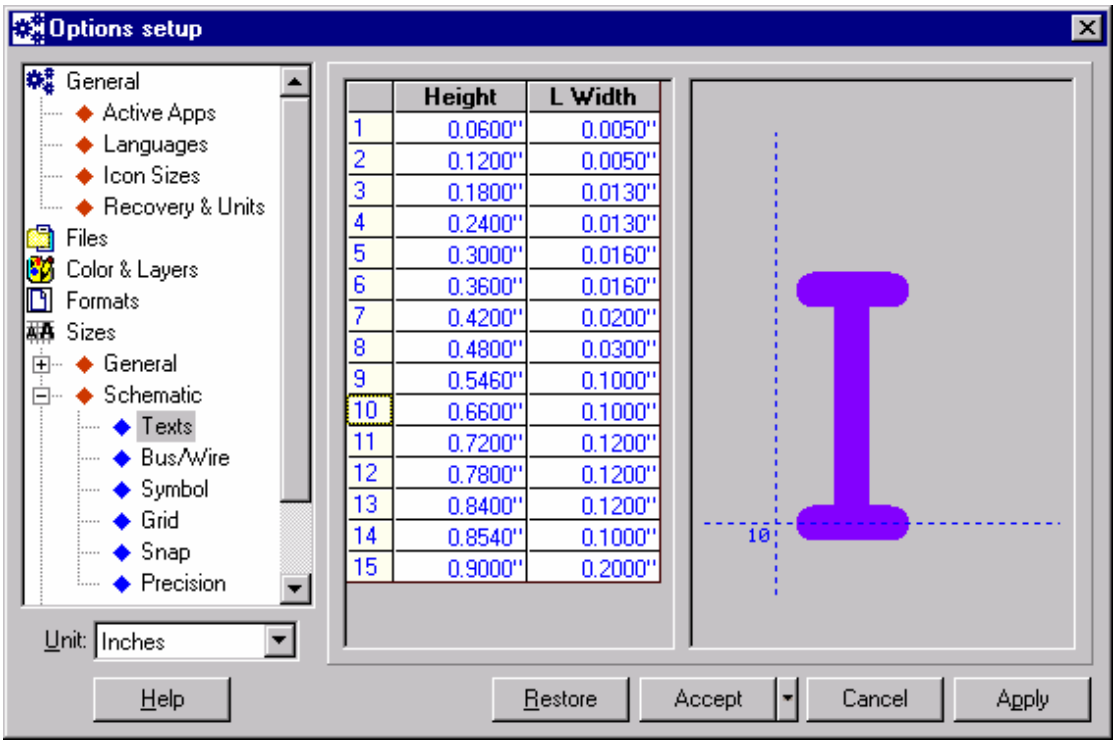


Fig: 2.10 Schematic option

Height: Allows setting the height of the text to a default value by selecting any one of the values given in the list box. The unit of measurement may either be inches or millimeters. New values may be entered in the text input box that pops up on double clicking the required column.

Line Width: Allows specifying the default line widths by selecting any of the values provided in the list box for any of the two units; inches or millimeters. Double clicking the required column opens a text box, where new values may be entered. This option is applicable to vector font only.

Bus/ Wire: Sets the default line widths for buses, wires and symbols. In the window that pops up, the sizes appear in editable text boxes. Double click the value to be changed, if necessary. This enables instant selection and edition of conductor sizes for created objects.

***Symbol Line widths*:** Allows selecting the line widths of the symbol, by entering new values to the input box that appears on double clicking the required row.

Grid: Allows setting the distance between the grids to any one of the given values. New values may be entered by double clicking the required row and typing the new value. The default values may be set to either of the two units, inches or millimeters.

Snap: Allows setting the minimum snap distance. Double clicking any row allows changing the current set values to new ones. The default values may be set to either of the two units, inches or millimeters.

Precision: Allows accuracy settings to be defined to the workspace by selecting any of the given values for zooming purposes. A set of new values may be chosen by double clicking on any one of the existing sets of values and typing in the new value. The default value selected may be set to either inches or millimeters.

Layout

Layout Text: Sets the height and line width of layout texts. A set of default values is displayed on selecting this. Double click on the values to make any change. The change is visible in the Preview part of the window immediately. Given below is a brief description of the parameters provided in the Fig.2.11.

Height: Allows setting the height of the text to a default value by selecting any one of the values given in the list box. The unit of measurement may either be inches or millimeters. New values may be entered in the text input box that pops up on double clicking the required column.

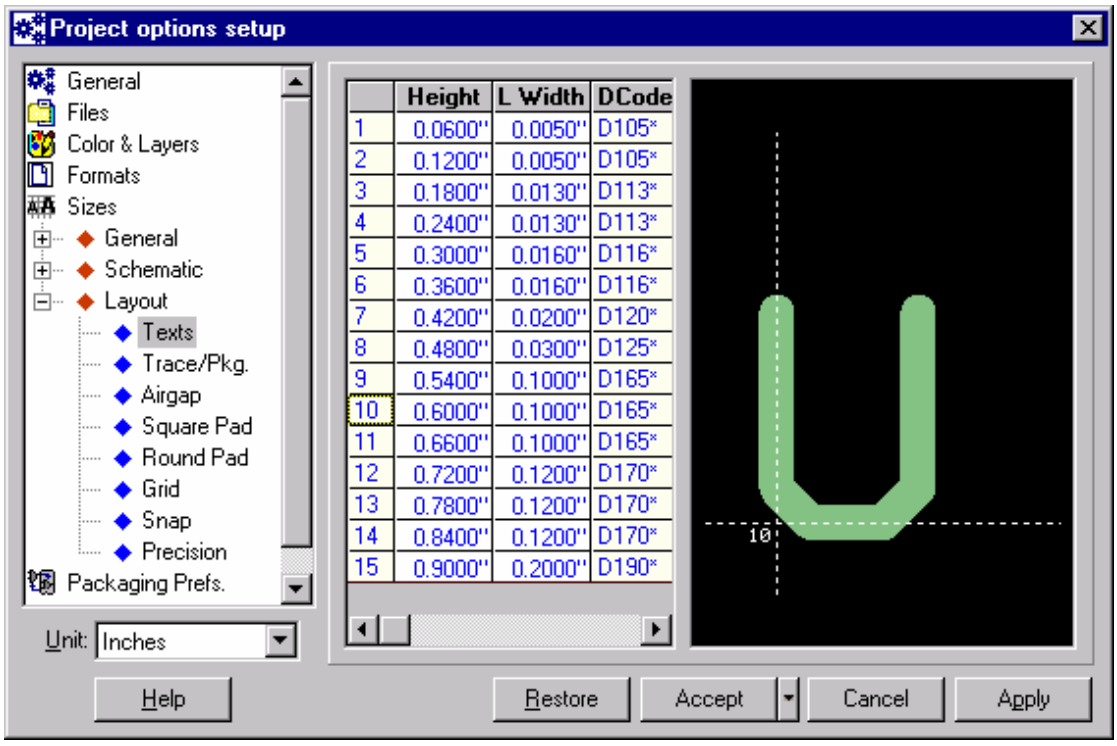


Fig: 2.11 Layout option

Line Width: Allows specifying the default line widths by selecting any of the values provided in the list box for any of the two units; inches or millimeters. Double clicking the required column opens a text box, where new values may be entered**.** This option is applicable to vector font only.

Similarly other parameters are as follows

Trace segment/ Package Line Widths/Round pad diameters/Square pad sizes: Sets the default values of trace segment/ package line width, airgap sizes, square pad sizes and round pad diameters. All sizes appear in editable text boxes.

Double click the value to be changed, if necessary. This enables instant selection and edition of conductor sizes for created objects. You can set the values of the given three parameters either in inches or mm. The default values may be changed in the input box, which pops up on double clicking the selected row.

Airgap size: Allows specifying the airgap between the traces and pads (round or square) in either inches or mm.

Packaging Preferences Option

These options when selected allow setting the global preferences for packaging of components. This window consists of three sections, each of which has been explained below.

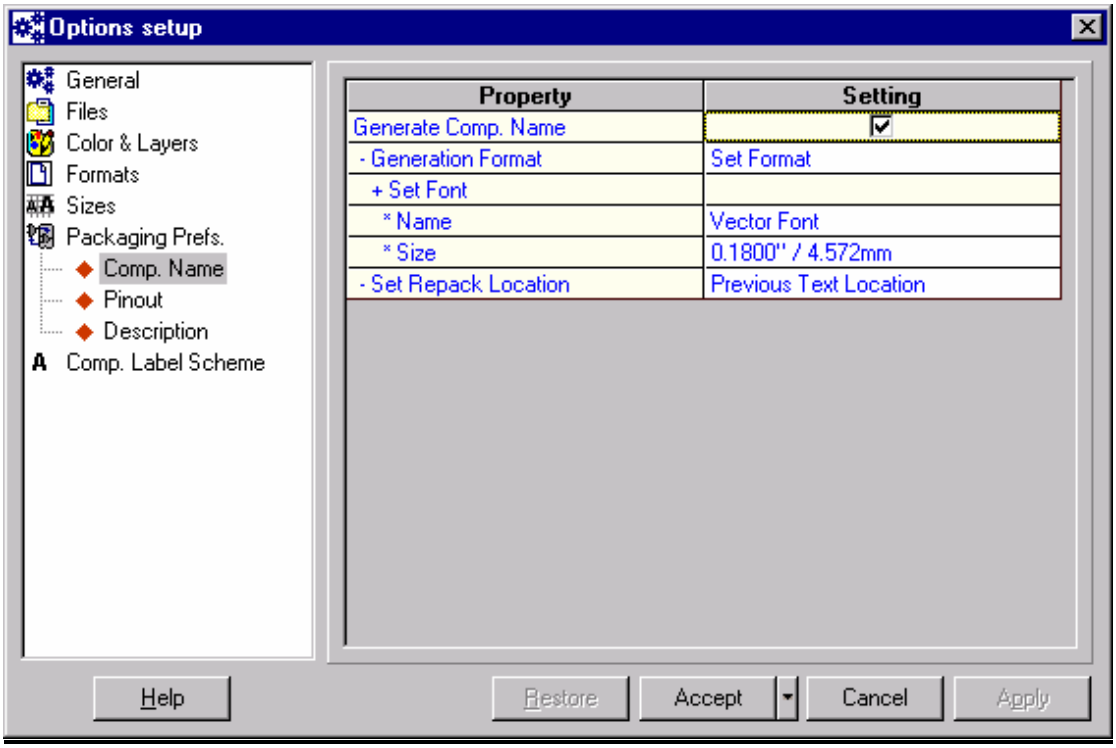


Fig: 2.12 Packaging Preferences option

Component Name:

Allow to set the generation of component name (U1, R1), default text font and text location with Repack function. Each of these options may be set either by selecting from their respective drop down lists or by enabling the checkboxes. The setting applies to all instances in the system where packaging of components takes place.

Given below is a description of each of the parameters that may be set in this tab.

Generate Component Name: Allows setting the packaging preference for generating component name by checking on it.

Generation Format:

Allows specifying the text size depending on the below mentioned two options.

> ***Predefined by symbol****:* This option allows specifying the text size as defined by the COMPNAME in the symbol.
>
> ***Set Format****:* Allows changing the default text size and font by choosing the values from a pull down list box.

Set Repack Location:

Allows setting the text location depending on the below mentioned two options.

> ***Previous text locations****:* This default option allows setting the text locations to the previously assigned location before repacking.
>
> ***Predefined by COMPNAME****:* Allows changing the default text locations by setting it as defined by the COMPNAME in the symbol.

Pinout:

Allow to set the options related to pinout text (package pin number). The options include generation of pinout text, text sizes, and text location with Repack function and Contents. Each of these options may be set either by selecting from their respective drop down lists or by enabling the checkboxes. The setting applies to all instances in the system where packaging of components takes place.

Given below is a description of each of the parameters that may be set in this tab.

Pinout Text: Allows generating the pinout text.

> **Predefined by symbol:** Allows generating the pinout text as predefined in the symbol.

Set format: Allows overriding the settings predefined in the symbol. 'Generate Pinout Text' checkbox option to override the packaging preference for generating pinout text. The other options are activated only if this is checked.

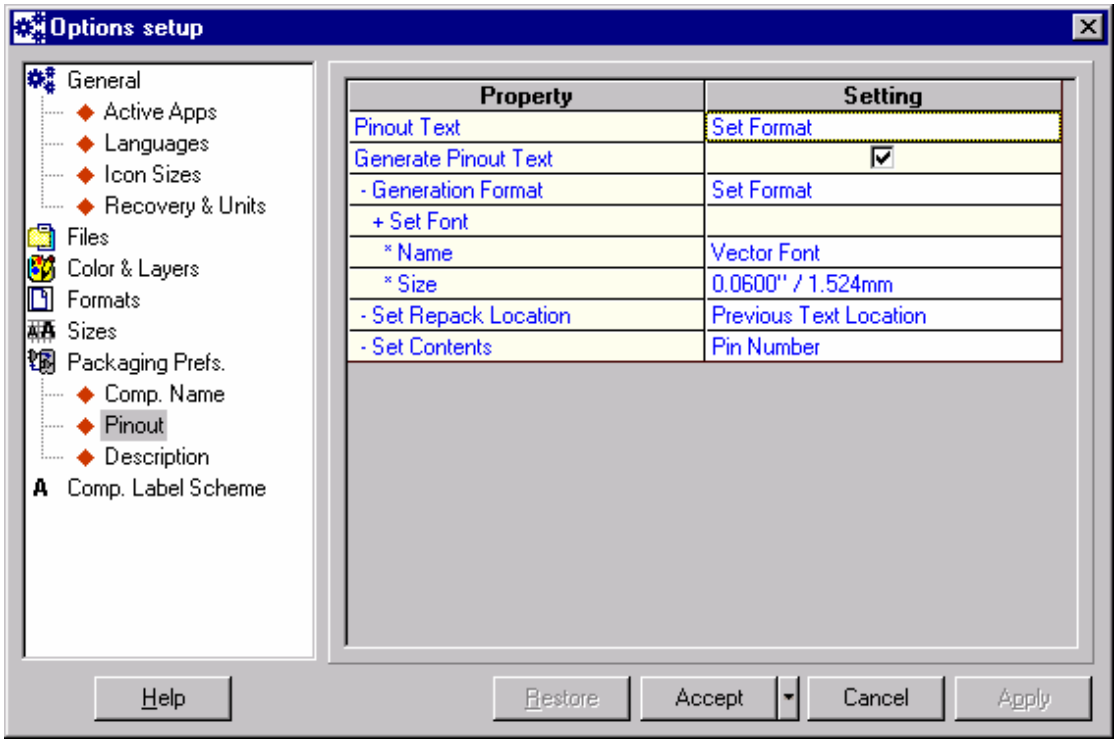


Fig: 2.13 Pinout option

Generation Format:

Default: Set the text font to default font.

Set format: Allows choosing the text font and size from the respective pull down list boxes.

Set Repack Location:

Previous text locations: Allows setting the text locations to the previously assigned location before repackaging. This is the default option.

Predefined by symbol: Allows setting the text locations as defined by the Pin Attribute text locations in the symbol.

Set Contents:

Pin Number: Allows setting the pin number to pinout text.

Entry Name: Allows setting the schematic entry names to pinout text.

Both Combined: Allows setting both the pin number and schematic entry name to pinout text.

Description:

Allows setting the options related to component description. The options include generation of part description, text sizes, text location with Repack function and Contents. Each of these options may be set either by selecting from their respective drop down lists or by enabling the checkboxes. The setting applies to all instances in the system where packaging of components takes place.

Given below is a description of each of the parameters that may be set in this tab.

Generate Part Description:

Allows generating the part description (7400, LM555). The other options are enabled only if this is checked.

Generation Format

Predefined by COMPDESC: Allows setting the text sizes as defined by the COMPDESC in the symbol. This is the default option.

Set Format: Allows choosing the text font and size from the respective pull down list boxes.

Set Repack Location:

Previous text locations: Allows setting the text locations to the previously assigned location before repacking. This is the default option.

Predefined by COMPDESC: Allows setting the text locations as defined by the COMPDESC in the symbol.

Set Contents:

The following Component Description may be set by checking the corresponding check box. Part Name, Part Full Name, External Index Code, EDSpice Reference, Group Name, No Group name and Group Name as Comp. Value.

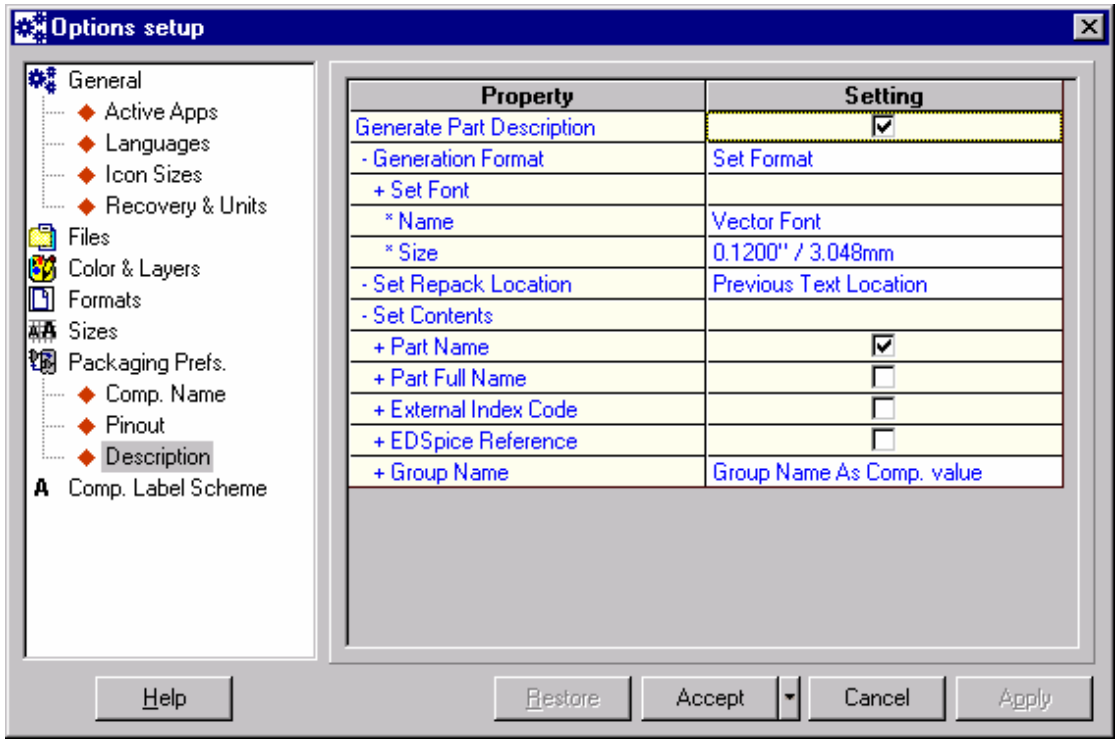


Fig: 2.14 Description Option

Components Labeling Scheme Option

This option when selected allows the user to set the labeling scheme for schematic/ layout components in the current project.
Each of the options may be set by enabling their respective checkboxes. Text font and size may be selected from the respective drop down list boxes (Similar to packaging preference).

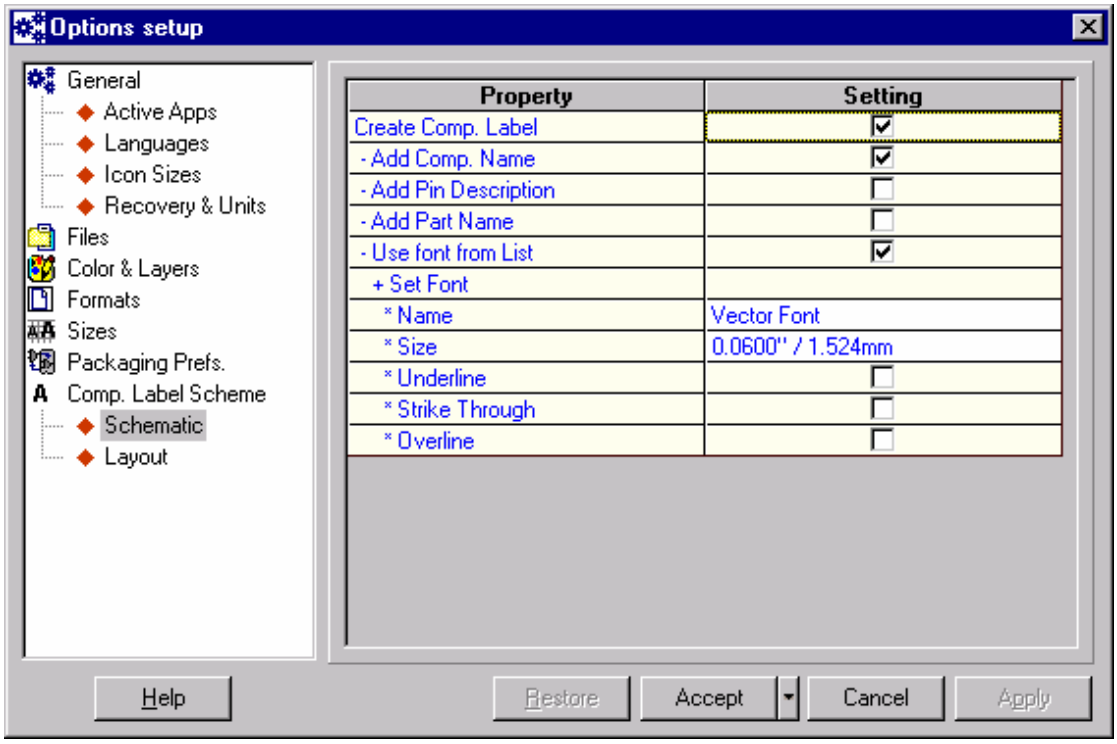


Fig: 2.15 Components Labeling Scheme Option

Aperture[1] Table Editor

The aperture table contains aperture sizes information that can be used to create Gerber data. These apertures are defined in terms of a format recognized by the photoplotter called D-Codes (draft codes). All the available D-codes and the sizes they represent are listed in Aperture Table. Artworks are generated with the help of photoplotters using specially shaped apertures through which light falls on the film in order to create a given shape on film.

The interpretation and repertoire of D-codes may vary depending on the make and model of the photoplotter. Latest photoplotters available in the market may recognize various D-codes for creating different shapes. EDWinXP defines three D-Codes for each available aperture size, namely for plotting lines, flashing round pads and flashing square pads, which are recognized by almost all standard photoplotters. All the available D-codes and the sizes they represent are listed in Aperture Table. Aperture table must contain only those D-codes, which the currently used photoplotter can understand.

The Aperture Table editor can be evoked from EDWinXP Project Explorer or from Fabrication Manager. The Aperture Table editor displays the current Aperture Table and a list of Aperture Tables used by certain standard photoplotters from which any Aperture Table may be selected as current. The apertures defined in the selected aperture table are displayed alongside. Custom. apt

[1] An aperture is an opening in a wheel through which light passed to expose the film.

provides apertures of all sizes from 1 mil to 330 mils with a difference of 1mil.The user may edit these aperture tables to suit his requirements.

System uses existing apertures to generate plotting data even for sizes not available in the aperture table. In this case, the system will use an aperture of the next lower size and then apertures of very small sizes to bring about the required shape and size (multistroking technique). The resulting files will be larger and the time required for generation of Gerber ASCII files and photoplotting may be considerably longer. Hence it is advised that as far as possible the sizes of pads and line widths should be limited to those covered by the aperture table

The Aperture Table may be invoked in the following two ways:

1. From task list in the project explorer.
2. From Fabrication Manager, select the menu Fabrication | Setup to invoke the dialog Fabrication Data Manager. Click on the category Gerber Photoplotter data. Set the Gerber Output Format to RS-274-D and click on the grid named Selected Aperture Table.

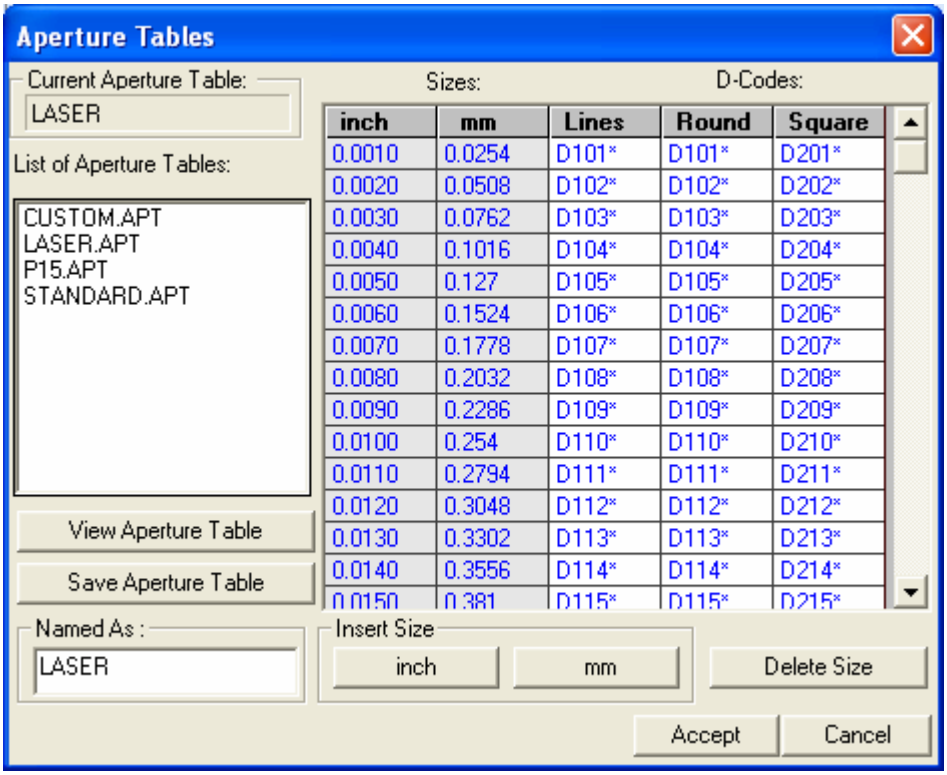


Fig: 2.16 Aperture Table Editor

Given below is a brief description of the Fig.2.16.

List of Aperture tables Provides a list of the aperture tables present, from which the required may be selected.

Current Aperture Table	Highlights the selected aperture table from the list.
Apertures	Provides a list of custom sizes and Dcodes of the selected aperture table in both inches and millimeters as the unit of measurement, the values of which may be altered.
Insert Size	Two buttons **INCH** and **MM** are provided, each of which may be clicked, to open an input box, where the new aperture size may be entered. The new value will be of the selected unit of measurement.
Named As	This text box allows entering new names to which the aperture table may be saved.
Save Aperture Table	Allows saving the changes made to the existing aperture table under the same or new name.

Click ***ACCEPT*** button for the changes to take effect.

Customizing the Aperture Table

Adding new sizes:	Select **INCH** or **MM** button, to specify the unit of measurement. An input box appears to enter new size. Enter the new size. Click ***Accept*** .Enter aperture code (D-codes) for Line, Round Pad and Square Pad in for this new size and save the changes. Note that the D-code must be terminated by asterisk (*) for ex: D200*.
Modifying D-Codes:	Select the required size from the Aperture Table by clicking on it. Redefine the D-Code of the selected aperture size and save the changes made.
Deleting Sizes:	Select the required size from the Aperture Table by clicking on it. Click ***DELETE SIZES***.

Aperture tables may be updated and saved under a different name. For this, give the name in the Named As text box and click ***SAVE APERTURE TABLE***. In this way, the user can retain the existing aperture tables while editing a copy of it.

Default Via Padstack Editor

This utility is used to set default parameters for a selected via Padstack (#1 to #16). A dialog box "Edit Via Padstack "opens listing all the layers. The via padstack may be selected from the dropdown list. The hole diameter may be specified in either inches or mm .The shape can be toggled by checking on shape field. Multiple selections can also be performed. To make any changes to the default values, click on the necessary field, the particular cell becomes editable.

Enter the necessary value and press Enter, this is important since if you directly move to another cell, the value of all the cells in between changes to the value of the previous cell. To change the shape, click on the particular cell and select the shape. Click on ***ACCEPT*** to save the changes made.

Given below is a brief description of the parameters provided in the Fig.2.17.

Select Via Padstack: Allows selecting the required via padstack from the drop down list. Depending on the via padstack selected, dimensions vary. The default via padstack selected is #1.

Airgap: Allows specifying the minimum electrical insulation that has to be provided for the pad. New values may be entered by typing in the required value in the text box provided. The default value set is 0.0300".

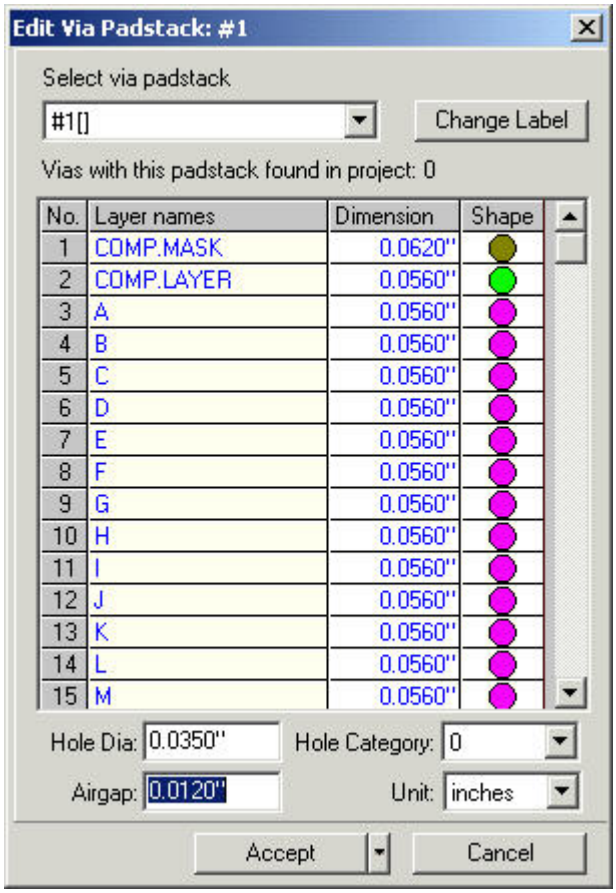


Fig: 2.17 Default Via Padstack Editor

Hole Category: Allows entering the category which assigns group holes into a maximum of eight categories (0 to 7) depending on their type. Category implies whether the hole is to be plated or not etc.

Layer: Displays the 28 copper and 2 mask supported by the system. Layers Component Print and Solder Print are not displayed.

Hole Diameter: Allows specifying the values for the hole diameter of the via.

Shape: Allows toggling the shape of the selected via for a particular layer to either round or square, the default being round.

After making the necessary changes, click ***ACCEPT*** button to save the changes. These default values may be changed from Layout editor.

Default Design Rules

This utility is used to preset certain parameters for manual, semiautomatic and automatic routing of traces and component placement. With the given parameters, the Layout conducts a design rule check and any problems are marked by an Error label. The errors may be queried using the Redraw| Error in Layout Editor. The design rule settings may be saved as a permanent setting or may be set for the circuit or for the current project only. The dialog box is as shown in Fig.2.18. And each of the parameters has been explained below. The parameters can be set as default for the application or individually for the particular project or circuit.

DRC System Setup

Routing layers & Direction (Applies to Layout Editor Only)

Not Used: If this option is selected the designer is not allowed to perform routing in this layer. A message box pops up prompting to switch to the allowed layer. Nevertheless user may use the option tool 'Place On Selected Layer' and switch to the layer, which has set to Not Used. After setting this option to NOT USED, user may validate the design for any design violation. This is done using the Layout Editor |Auto| Autocheck| Check Other Violation tab. In this tab check 'Traces on Wrong layers'. The results are displayed in the Design Rule Violations dialog. Click on the right side row to display the description of the error. When clicked on each error, the error portion is highlighted on the workspace.

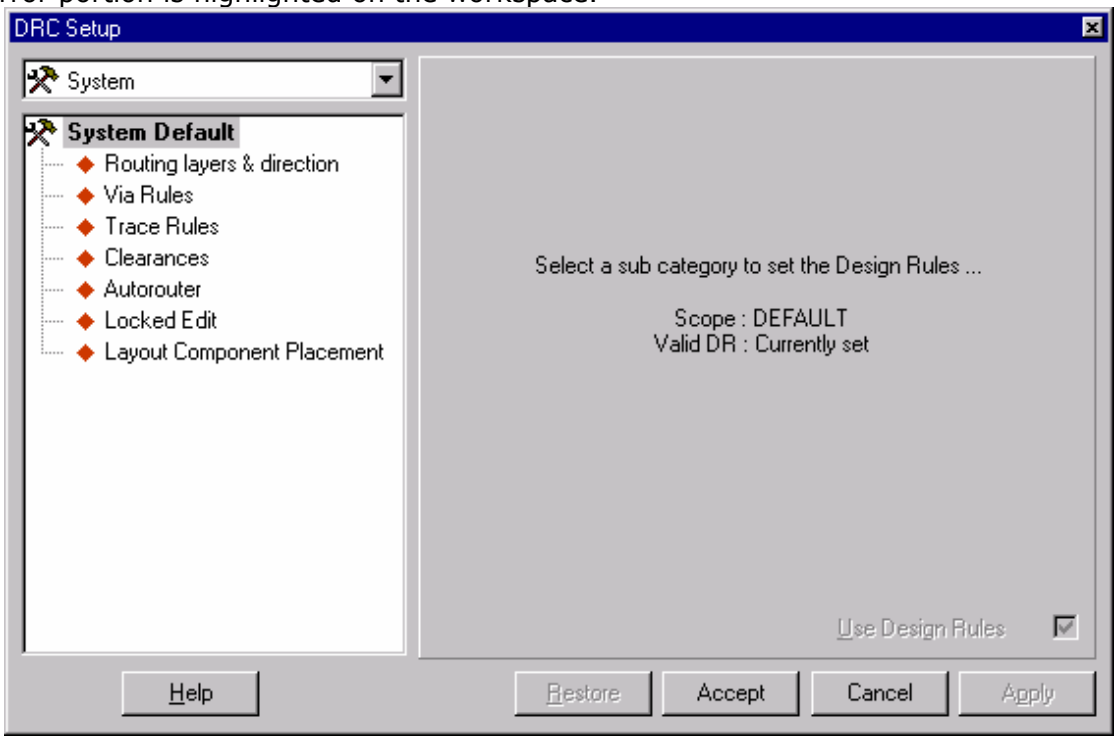


Fig: 2.18 DRC Setup- System

Horizontal or Vertical: Set the required direction and check the option Traces routed on wrong direction in Autocheck window (Layout Editor |Auto | Autocheck| Check Other Violation tab). Execute the operation to display the results in the Design Rule Violations dialog window. Click on the right side row to display the description of the error. When clicked on each error, the corresponding error is highlighted on the workspace.

Via Rules

Via allowed: Allows to specify whether via padstack can be used in the design or not. If not specified, system displays the violation error when Autocheck (Layout Editor| Auto |Autocheck| Check Other Violation tab) is performed provided the option Layer Change Through Via Hole is checked.

Maximum number of Vias per Trace: Permits the user to specify the maximum number of vias allowed on a trace connecting between component Pads. If the number of via padstack used is more than the number specified in DRC dialog, system displays the violation error when Autocheck (Layout Editor| Auto | Autocheck |Check Other Violation tab) is performed provided the option against Too many Vias on Pin to Pin Connections is checked.

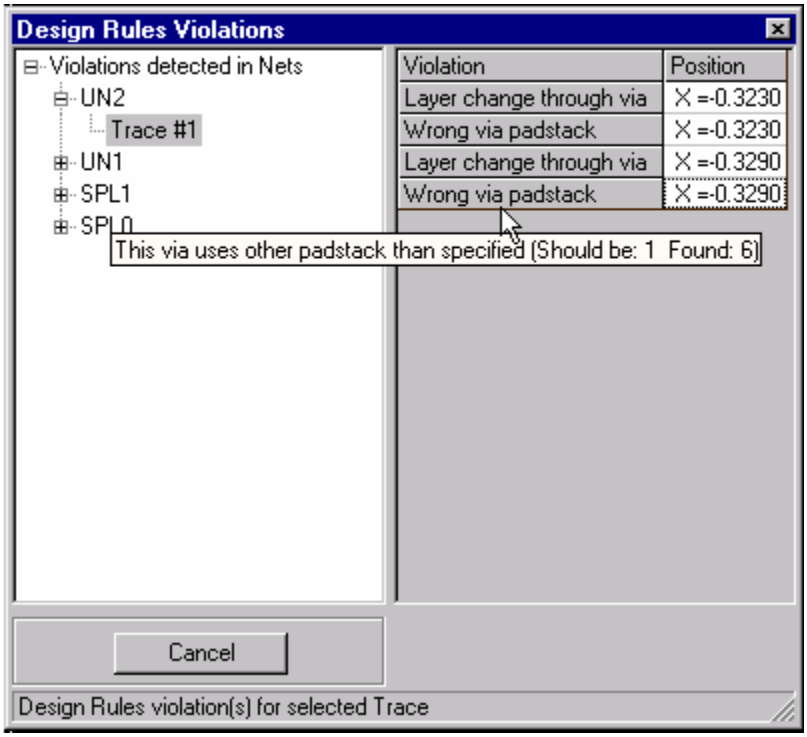


Fig: 2.19 DR Violation for Selected Trace

Trace Rules (Applies to Layout Editor Only):

This option allows setting the required trace parameters such as trace width, trace airgap, and the trace length. The value of certain trace parameters may be selected from the given list or may be specified. If any of these settings is violated, system

displays the violation error when Autocheck (Layout Editor |Auto |Autocheck |Check Other Violation tab) is performed provided the required option under Trace Rules is checked. The errors are displayed in the DR Violation dialog as shown in Fig.2.20.

Clearances (Applies to Layout Editor Only):

This option allows to set the clearances between Trace to Trace, Pad to Pad, Pad to Trace and Single Trace Check Width. To check any violation in the design, run the Autocheck (Layout Editor| Auto| Autocheck| Check Clearances tab). To use the Design Rules settings, check Use Clearances as in Design Rules for Layers. The error labels are displayed on the design. Each error labels signify the type of error encountered.

Autorouter (Applies to Autorouter Only):

The settings for the Arizona Autorouter may be set in DRC dialog. The settings include Fanouts routing enabled, Trace routing enabled, SMD connection only, Number of routing axis, Wrong layer direction cost, Wrong direction optimizing cost, Right direction optimizing cost and Vias Optimizing cost. These settings may also be set in Arizona Autorouter however, to use DRC settings check the necessary options in the Arizona autorouter. The options available in Arizona are

- Use these settings if not explicitly specified in Design Rules: Allows to use the settings specified in Arizona if the settings are not explicitly specified in DESIGN RULES.
- Override setting specified in Design Rules: Allows to override the settings set in DESIGN RULES.

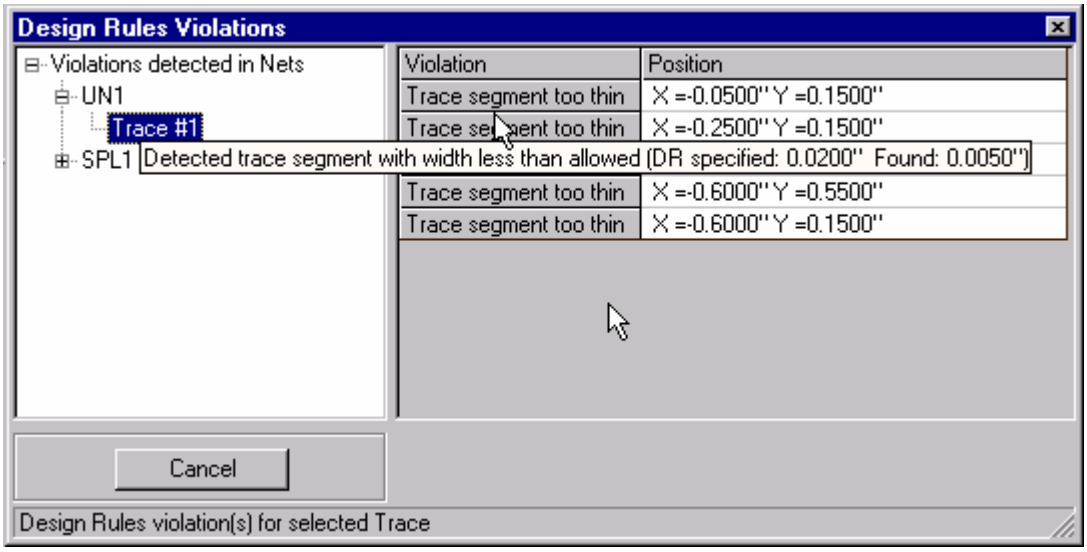


Fig: 2.20 DR Violation Dialog

Locked Edit (Applies to Layout and Schematic Editors Only):

This option is applicable to both Layout and Schematic editor. Certain operations related to Nets, Nodes, Pin Swapping, Adding/ Deleting components may be locked

by enabling the check boxes. The option set prompts the user of rules violations thus prohibiting the user to violate the rule.

Layout component Placement (Applies to Layout Editor Only):

The options listed here are explicit to layout components. The parameters include component orientation, name placement, name orientation, component name distance, component snap, distance to surrounding layout components and check distance while placing. The option set prompts the user of rules violations, thus prohibiting the user to violate the rule. The Layout Component Snap works a slight differently. Follow the description given below.

Component Snap (applicable to layout only): The component snap value can be set in the layout module and in Design Rule Check dialog. The snap value set in Default Design Rule dialog has higher priority over the value set in layout editor.

Operation: Snap values are listed in the Snap text box. The required value may be selected from the down list box or manually entered in the text edit box provided. When unit (View | Unit) is switched between inches and millimeters, the value in Snap changes accordingly.

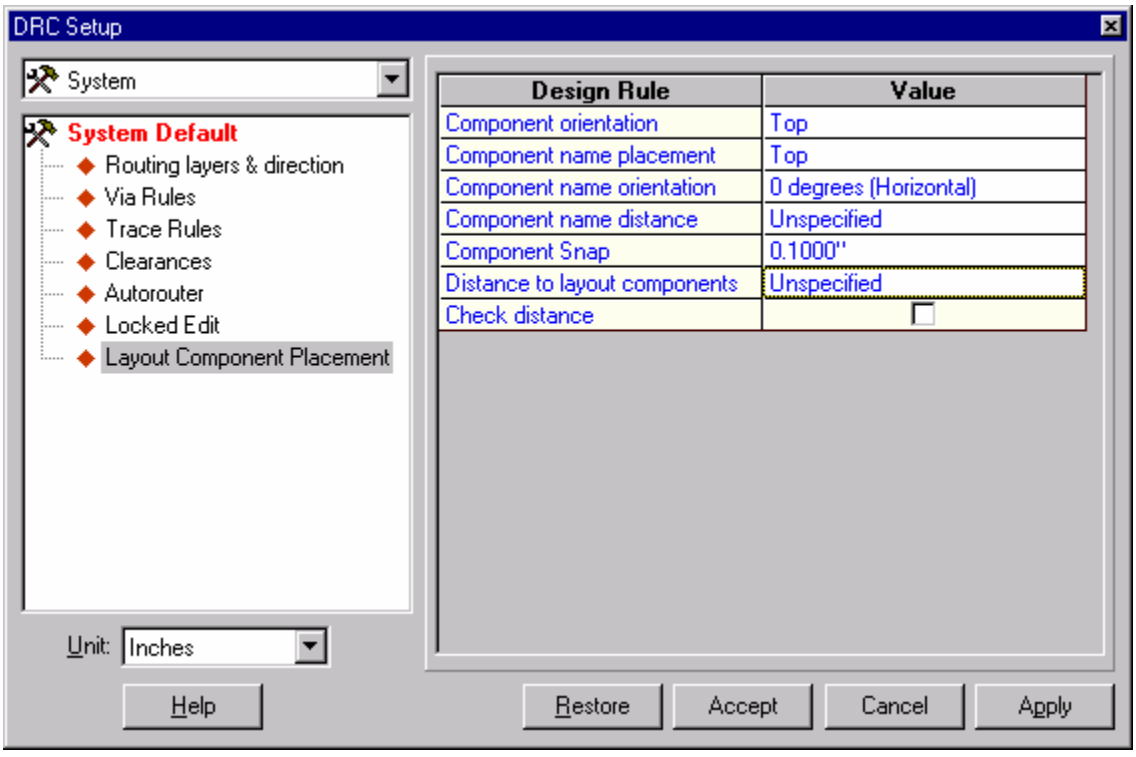


Fig: 2.21 Layout Component Placement

How to use an alternate Snap value (for Layout Components only) using design rule setup dialog?

Open Design Rule dialog from EDWinXP Project Explorer and enter the snap value say .1000” in Layout component Placement. In Layout Editor, set the snap value to .0500”. Now try relocating the components, you may find that the components move with Snap value .1000”. To use the Snap value selected in Layout editor, press CTRL key and try to relocate. Now the Layout Components move with Snap value .0500”.

DRC Project Setup

In the drop down menu of DRC setup dialog box select **Project [Untitled].** This allows presetting certain parameters for manual, semiautomatic and automatic routing of traces and component placement. The explanation of different parameters that can be set using the DRC Setup dialog for a particular project are similar to that in the **DRC System Setup**.

DRC Circuit Setup

In the drop down menu of DRC setup dialog box select **Circuit [MAINHIER].** This allows presetting certain parameters for manual, semiautomatic and automatic routing of traces and component placement. The explanation of different parameters that can be set using the DRC Setup dialog for a particular project are similar to that in the **DRC System Setup**.

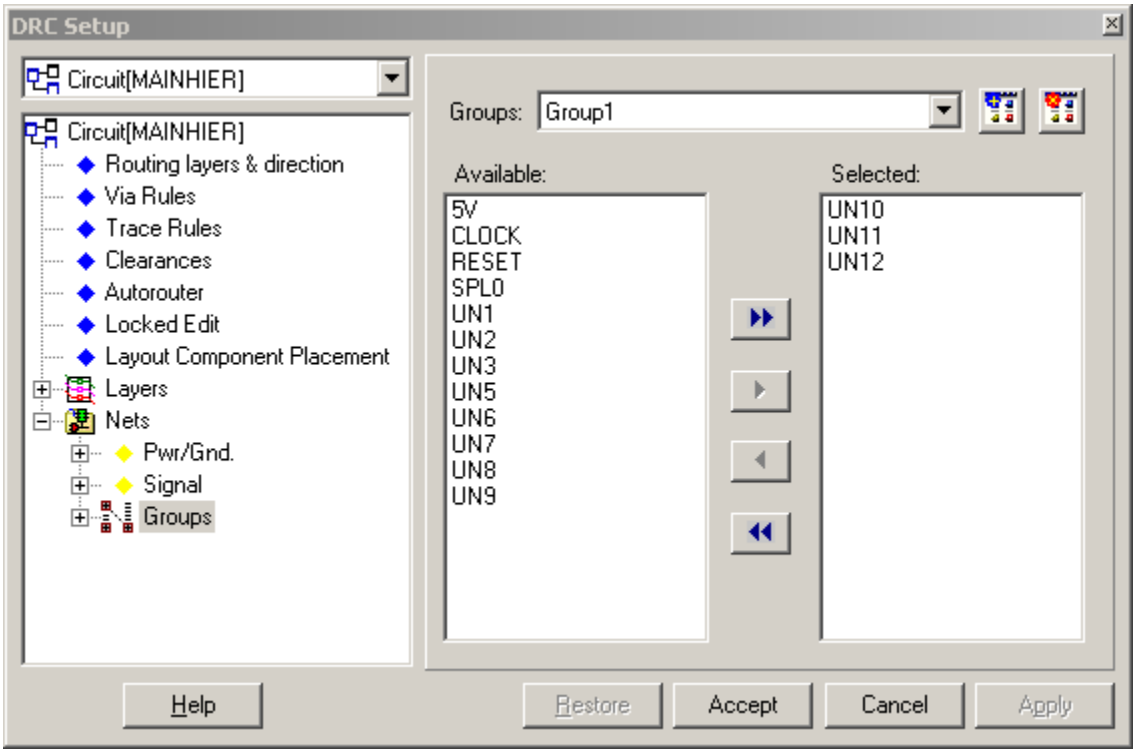


Fig: 2.22 DRC Circuit Setup

Given below is the explanation of the additional parameters that can be set in the dialog box given in Fig.2.22.

Layers: Different set of Trace Rules and Clearances values may be set for individual layers.

Nets: This is a sophisticated option, which allows to set different parameters for PWR/GND or Signal lines. Also the signal nets may be again grouped and different set of parameters may be set.

How to group nets?

Select **GROUPS** from the tree structure and click on ***ADD GROUP*.** Enter the name of the group say Group1. Now select the nets from the displayed list and click on  or  to move the selected nets to the list box. Any number of Groups may be created. The added groups are displayed in the tree structure and may be deleted using **DELETE GROUP**.

These settings when handled cautiously and cleverly can help you to design an error free board. The settings can, not only be made default but also be made for the current project or current circuit.

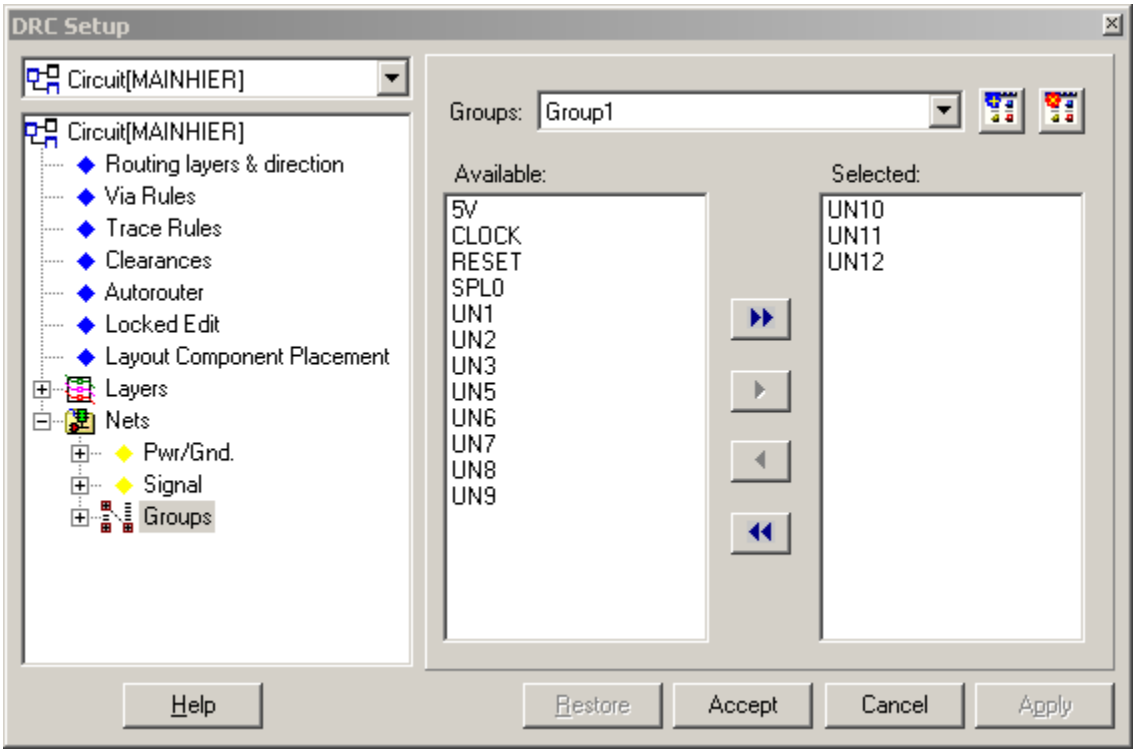


Fig: 2.23 Grouping Nets

Conversion Manager

Conversion Manager is used for converting the libraries, databases of EDWin 16-bit compatible to EDWinXP and, EED III Conversion.

Library Conversion

To convert the Libraries of EDWin 16-bit to EDWinXP Libraries, select the **LIBRARY CONVERISION** tab. set the EDWin Library path for conversion. The Library Elements will be listed in the window as shown in Fig.2.24.

To convert the Libraries, click on the corresponding Library Elements. Libraries with their extensions will be displayed in the box below. From the list select the Library Element for conversion. The items in that particular Library will be listed in the box beside. Multiple selection is also possible for conversion.

Select the item to be converted and click on the ***CONVERT*** button. A window, *Save Library* pops up.

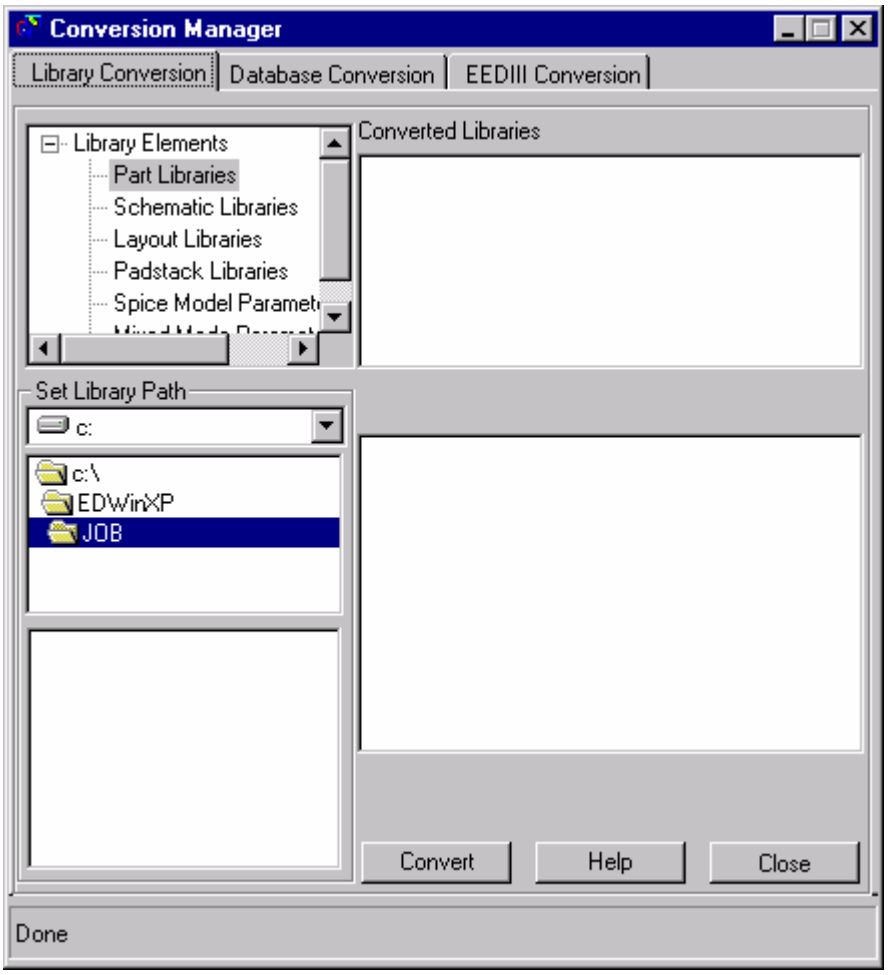


Fig: 2.24 Conversion Manager

Set path to save the Library .The file name with the modified extension is displayed in the box below. Click ***SAVE*** button to save the Library Element. In Conversion Manager window the path with the Library name will be displayed in the Save As dialog box.

Importing old libraries and database (Projects)

Using EDWin16 libraries and databases: All EDWin16 bit databases and libraries should be converted to EDWinXP format using Conversion Manager.

A library element in EDWinXP format contains additional fields for storing cross-references. These cross-references are not needed for proper functioning of the system but are useful for searching and browsing. Since this information cannot be reconstructed automatically during conversion, a special program called Field Editor has been provided. Certain cross references required for proper functioning of Library Browser and Library Explorer will be updated automatically when library file is passed through Field Editor. For example: in EDWin16 thermal parameters were kept in separate files (.DAT/ .TAL). Now all this data is stored within the respective Parts. Field Editor also enables to add other necessary information (manufacturer name, type etc) in manual edit mode.

In EDWinXP, when you try to save old DEVICES or PARTS taken from old DATABASES, it is required that you have to save the corresponding symbols and packages used by the Parts into User Libraries (and of course subsequently included those files into the Search Sequence).

Using EDWin32 Libraries and databases: All EDWin32 libraries and databases are upward compatible and for usage with EDWinXP need not be converted but they need to be updated using Field Editor.

Database Conversion

To convert the databases of EDWin 16-bit to EDWinXP, select the **DATABASE CONVERSION** tab. Set the path for the database to be converted. The list of databases will be displayed in the box beside.

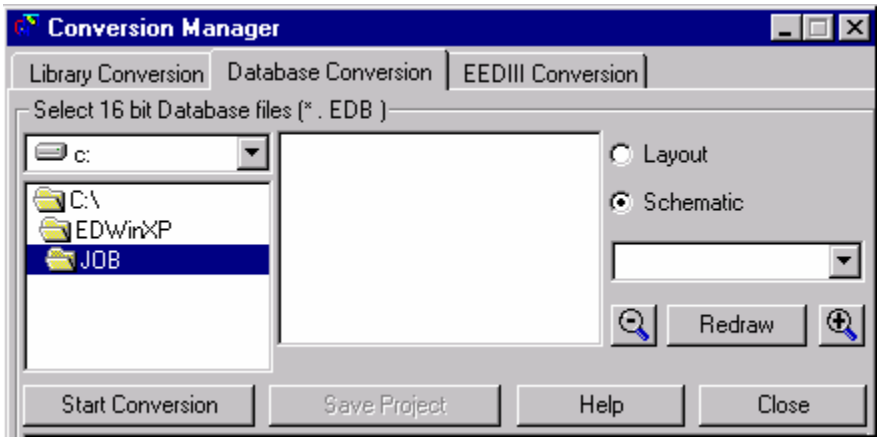


Fig: 2.25 Database Conversion

From the list double click on the database to be converted. The database gets displayed in the main window. The Schematic or Layout representation may be viewed by selecting the corresponding option buttons.

To start the conversion click ***START CONVERSION*** button. When conversion to EDWinXP is complete a confirmation box pops up. Click ***Yes*** to save the database. A Save As dialog pops up. Select the path and click the save button. Thus the 16-bit database will be converted into EDWinXP Project database.

EEDIII Conversion

Library

This option helps to convert EEDIII Libraries saved in ASCII format to EDWinXP libraries.

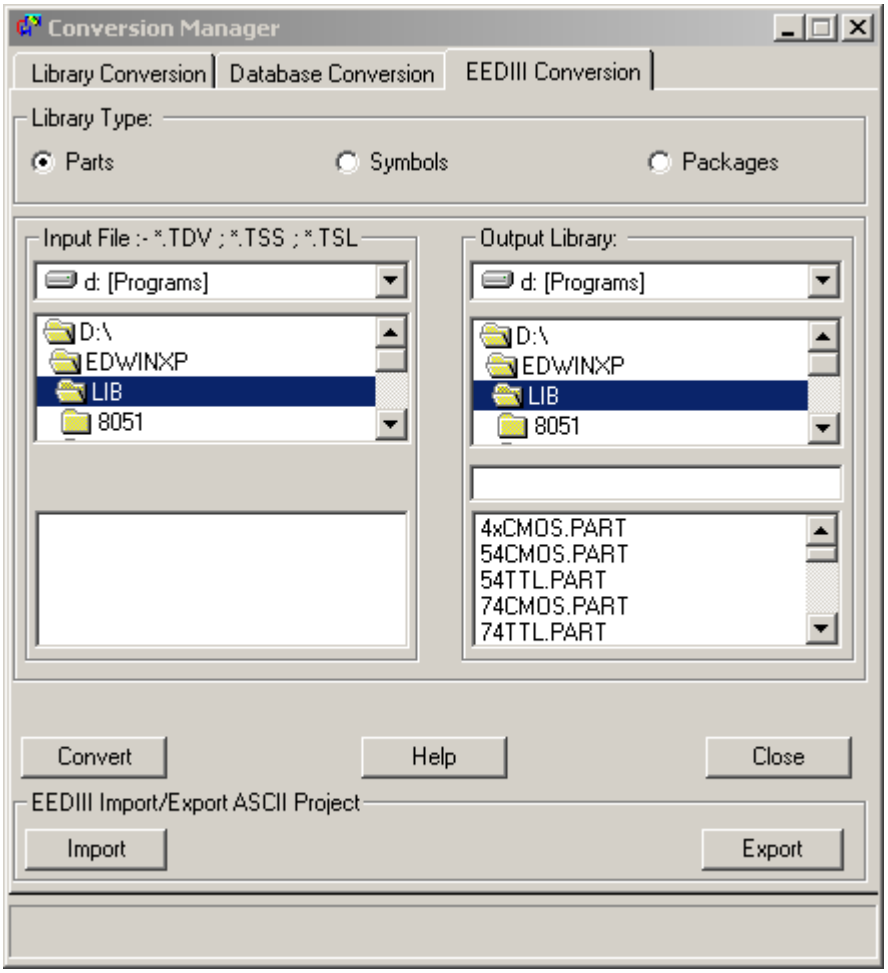


Fig: 2.26 EEDIII Conversion

Any Library type (Part/ Symbol/ Package Libraries) may be chosen by enabling the option buttons. The extensions for files are *.TDV/ *.TSS/ *.TSL for Part/ Symbol/ Package Libraries. The EEDIII files are selected by selecting the file from the input file box. In output Library, the path is selected to save the conversion. Click ***CONVERT*** to convert the selected file to EDWinXP Libraries. To exit this window click ***CLOSE***.

Database / Project

For conversion of EEDIII database to EDWinXP ASCII database and vice versa Import/Export facility is provided in EDWinXP Conversion Manager Window. EED III Project files (schematic & layout) saved in ASCII format could be imported to EDWinXP

EEDIII to ASCII Project Conversion

This routine converts EE Designer III (ver 2.4 or later) to EDWinXP. Conversion may be executed by importing EE Designer ASCII databases. Due to differences in structure and contents between EED and system databases certain restrictions apply.

Starting EEDIII to ASCII Project Conversion:

- Right click System and select ***Conversion Manager*** from the list. Now select the third tab EEDIII conversion and click on Import.
- Select ***Conversion Manager*** from the task list or from the task toolbar. Now select the third tab EEDIII conversion and click on Import.

The EEDIII TO ASCII Project Conversion window appears as shown in Fig.2.27.

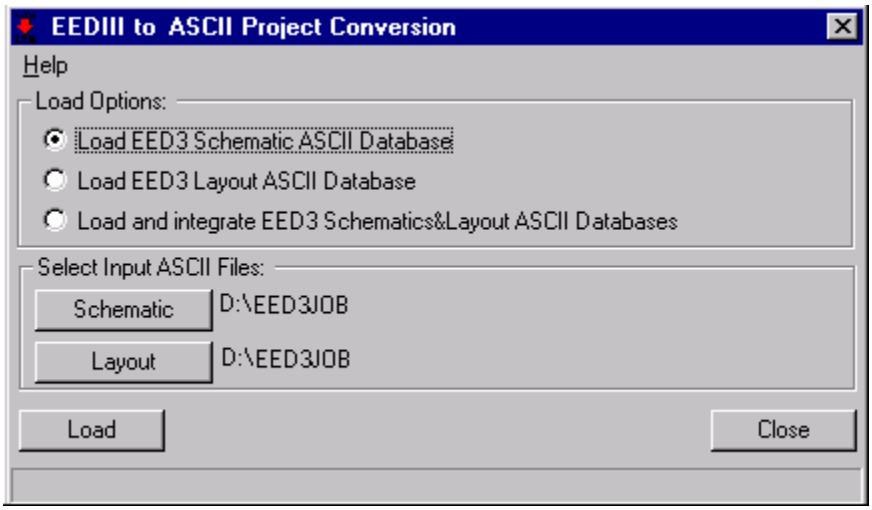


Fig: 2.27 EEDIII TO ASCII Project Conversion

Load EED3 Schematic ASCII Database: This option helps to Import schematic ASCII database. Select this option from EEDIII to ASCII Project Conversion window and click Schematic. A dialog box pops up from where the file to be loaded can be selected.

Load EED3 Layout ASCII Database: This option helps to load the layout ASCII database. Select this option from EEDIII to ASCII Project Conversion window and click Layout. A dialog box pops up from where the file to be loaded can be selected.

Load and integrate EED3 Schematic & Layout ASCII Databases: This option helps to Import and integrate schematic and layout databases. Select this option from EEDIII to ASCII Project Conversion window and click ***LOAD*.**

Schematic: Select this button to load the EED3 Schematic ASCII database to be converted. A window Select EED3 Schematic ASCII Database to Load pops up. Select the required file (*.asc file) and click ***OK***.

Layout: Select this button to load the EED3 Layout ASCII database to be converted. A window Select EED3 Layout ASCII Database to Load pops up. Select the required file (*.ala file) and click ***OK***.

Load: Allows to load the symbols and packages of the selected ASCII files. When invoked, system reads the selected ASCII file and prompts for saving to a file *.EPB. Two more buttons are made visible at this juncture, ***SAVE*** button to save the database and ***VIEW*** button to view the converted EED3 database.

EED3 ASCII Database Conversion

EED3 ASCII Database Conversion is a utility that converts schematic diagram and/ or PCB layout design of a selected project to ASCII files in a format acceptable to EE Designer. The basic difference between the database concepts of the two E-CAD systems is that though the circuit database in EE Designer may be integrated by front and back annotation, it is contained in two disk files - one for schematic diagram and one for PCB layout of the circuit. Each part may be stored and loaded from respective ASCII files with the file name extension .ASC for schematic diagram and .ALA for PCB layout.

Starting EED3 ASCII Database Conversion

- Right click System task in Project Explorer and select ***Conversion Manager*** from the list. Select the third tab EEDIII conversion and click on the EXPORT button.
- Select ***Conversion Manager*** from the task list or from the task toolbar. Select the third tab EEDIII conversion and click on the EXPORT button.

The EED3 ASCII Database Conversion window appears as shown in Fig.2.28.

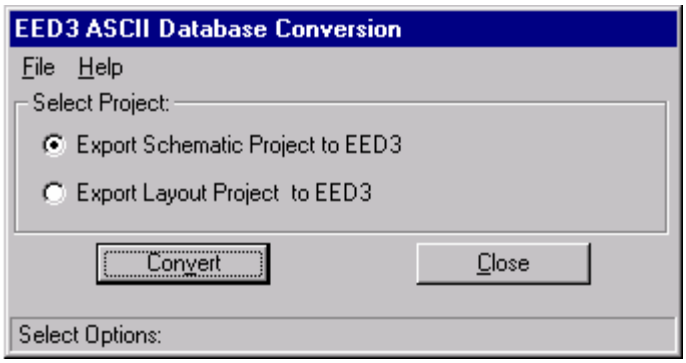


Fig: 2.28 EED3 ASCII Database Conversion

Export Schematic Project to EED3: This option allows to convert the Schematic diagram of the selected Project to ASCII files in a format acceptable to EE Designer.

 *Since the EED simulators are very different, the simulation parameters are stripped from converted symbols.*

Line sizes: Line sizes of graphic items and texts in symbols, design notes and page notes are not recognized in EED schematic diagrams for entities other than bus segments.

Export Layout Project to EED3: This option allows converting PCB Layout of the selected Project to ASCII files in a format acceptable to EE Designer.

 *There may be some limitations when converting the PCB layout of the Project to EED3 format.*

Layer mapping: EED recognizes only 12 layers while the project may have 30. Therefore, before conversion all trace layers used in the project must be mapped to layers of EED. Traces placed on unmapped layers will appear on the COMP. PRINT layer in EED.

Line sizes: Line sizes for graphic items placed on COMP. PRINT and SOLD. PRINT layers are converted to .001". For items placed on the trace layers, line width should not exceed .255". Same applies to the width of trace segments.

Padstack conversion: Padstacks for round and square pads (pin mounted devices) will be properly converted if the size does not exceed .255”. Same applies to hole diameters. Arcs and circles in padstacks for SMD pads will be ignored.

Copper planes: Copper plane items may be assigned to a maximum of 8 different nets. Circles are ignored.

Converting parts: To output part description in formats acceptable to EED, the system needs to access package(s) referenced by the part. If such package(s) are not available in the local library, the corresponding part will not be converted.

Convert: This button is used to execute the conversion of project to EED3 ASCII database file. Select one of the options depending on whether the schematic or layout is to be converted and click ***CONVERT***. In the case of layout, this pops up a *Conversion Setup* window that allows to map all trace layers used in the project to layers of EED. The list of all the layers of EED is displayed in the window. Click on the required EED layer from the list and then in the column under EED Layers: next to the layer in the project that is to be mapped to the selected EED layer. There is also an option to convert the arc segments to lines. After the mapping is completed, click ***ACCEPT*** to pop up an EED3 - ASCII Database File Name: window where the name of the ASCII file to which the database is to be converted is entered. By default it displays the database name with the extension .ALA. In the case of Schematic, clicking ***CONVERT*** pops up an *EED3 - ASCII Database File Name* window where the name of the ASCII file to which the database is to be converted is entered. By default, it displays the database name with the extension .ASC. Click ***OK*** to execute

the conversion. When the conversion is completed, the message bar displays the message *Conversion completed OK*.

Subcircuit Adapter

The Subcircuit Adapter allows existing SPICE subcircuits to be converted into an EDSpice format, that is, a header is added to the subcircuit as SPICE comment lines. This allows a subcircuit to be assigned to a symbol in the Interactive Module, while maintaining compatibility with any other version of SPICE.

Starting the Subcircuit Adapter

This module may be invoked from Project Explorer in the following ways.

- Right click **System** and select ***Subcircuits Adapter*** from the list.
- Select ***Subcircuits Adapter*** from the Task list or from the Task toolbar.

File

This menu item allows the following file operations.

Open*:* Allows to open an existing SPICE netlist file (*.cir) and also files of *.lib**,** *.prm, *.fam, *.mod, *.spi formats. Here multiple files can be opened at the same time.

Save In*:* Allows saving the currently loaded subcircuit file (*.sbc) to a different directory. Select the directory for saving the currently loaded subcircuit file (*.sbc). After selecting the directory, select Save Subckt to save.

Save Subckt*:* Allows to save the subcircuit. Save the subcircuit to a selected family available in the directory / Eds_SBK. Either the subcircuit may be grouped into a new family or may be saved to the existing one. No special characters are allowed for the family name. The name of the file is made up from the name of the subcircuit appended with the extension .SBC.

Edit

This menu item allows the following editing operations.

Apply: To accept the description given to the Nodes and generate the subcircuit file with the added strings.

Previous File*:* In case where multiple files are opened, this option allows to switch to the file previously opened.

Next File: In case where multiple files are opened, this option allows to switch to the next file.

Converting and Saving Subcircuits to be used with EDSpice

- Select File| Open to open the required SPICE netlist file *.cir file. The selected SPICE netlist file is displayed as shown in figure below.

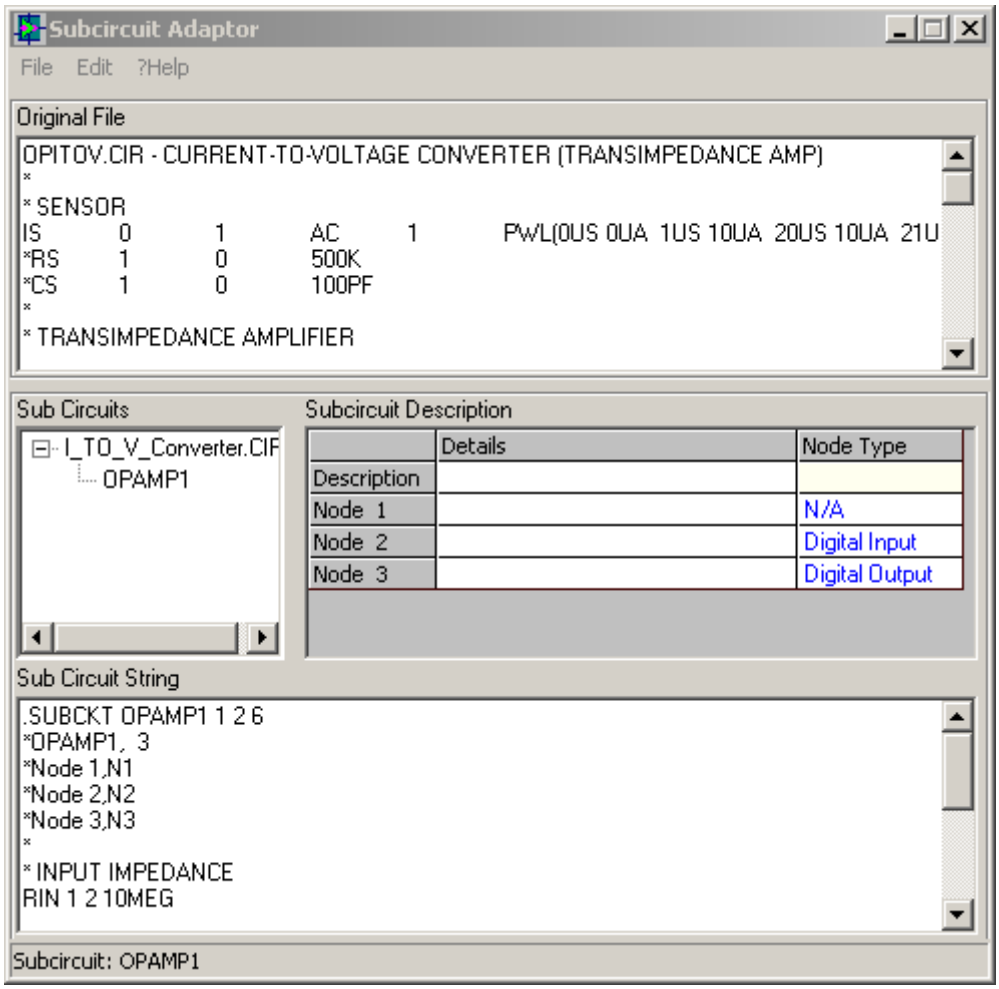


Fig: 2.28 Subcircuit Adapter

Subcircuits currently available, in the opened file, will be listed in the window Subcircuits. The list will also show the hierarchical relationship between subcircuits, that is, a tree-like structure displaying which subcircuits call the other subcircuits i.e. nesting.

- Select a subcircuit from the list by clicking on the name of any subcircuit displayed in the window Subcircuits.
- It is a must to supply a description for the subcircuit including one for each of the available nodes. The description for each node is typed into the edit box called Node Description. The column 'Node Type' allows selecting the node type for the subcircuit. Digital input and digital output nodes can be selected from the dropdown. When this subcircuit is used in a circuit, if required EDSpice will automatically insert proper bridges to the nodes after checking

this node type. After giving the proper descriptions, select Edit/ Apply. You can view the file with the strings that are added, in the display window Subcircuit String.

- Save the subcircuit from File menu. Save the subcircuit to a selected family available in the directory / Eds_SBK. Either the subcircuit may be grouped into a new family or may be saved to the existing one. No special characters are allowed for the family name. The name of the file is made up from the name of the subcircuit appended with the extension .SBC.

Creating Index: This option is available in Edit menu, It allows to create a library index file (.IDX) containing the information of all the subcircuits. This enhances the Speed of Building Spice Subcircuit Library References at the loading time of EDSpice Simulator. On selecting this option, a building process takes place and stores the created library index file in .IDX file. The default path is drive: / Eds_sbk.

Model Parameter Editor

The Model Parameter Editor eases the management and creation of model libraries. It can be used in a variety of ways including extracting .MODEL lines from existing SPICE netlist, loading existing models from the model libraries allowing you to modify and re-save them, and the creation of new models.

Starting the Model Parameter Editor

This module may be invoked from Project Explorer in the following ways:

- Right click System and select ***Model Parameter Editor*** from the list.
- Select ***Model Parameter Editor*** from the Task list or from the Task toolbar.

By default, the task toolbar will not be displayed. It may be enabled from View menu in the Project Explorer.

File

Open Model Parameters Library: Opens an existing model parameter library. Select any model from the list 'Model '. The parameters of the selected model are displayed in a table. Click on the column 'Value' to edit the values corresponding to the various parameters. Select File/ Save Model to update this file.

Load Model Templates: Loads the model templates available. Select the required template model. You have to supply a model library ID, from which the model library name for this model is generated, and a comment/ description about the model. Enter the values for the various parameters by clicking on the column 'Value' to get the edit box. After setting the parameters, save the model to an existing model parameter library or to a new library.

Extract from Netlist: Loads the parameters already stored in the circuit file (as .model line).Select any .model line to list out the parameters in the table below.

Enter the Model Id and the Comment. Edit the values, if required, for the various parameters by clicking on the column 'Value' to get the edit box. After setting the parameters, save the model to an existing model parameter library or to a new library.

***Save Model**:* Saves the model with the set parameters.

Edit

Find: Allows searching for a particular model in the library.

Delete: Allows deleting the model selected from the library*.*

Recreate Model Parameters Library Index: Allows to Recreate Model Parameter Library and stores in Library Index file (.IDX). This, enhance the Speed of Model Parameter Library references at the loading time of EDSpice. Select Recreate Model Parameter Library Index after making necessary changes to the Model Parameters. A building process takes place and stores the recreation in .IDX file. The default path is /EDWinXP folder.

Creating New Models

First select the type of template for which you want to create a model from the list of templates displayed in the section 'Model'.

On selecting a template; the type of model, description of the model and list of the available parameters are displayed. To edit any of the parameters just click on the cell 'Value' to get the edit box. Change the value and press the ENTER key on your keyboard to accept the new value.

Once you have finished editing the parameters select File/ Save Model to save the model. You have to supply a model library ID, from which the model library name for this model is generated, and a comment/ description about the model. You can either select an existing library file to save this model into or specify a new file name.

Loading Existing Models from a Library File

Select File/ Open Model Parameters Library. From the Open Library window, select a model library file by clicking on the name of the file you want from the list supplied. A list of model names will then be displayed. Once you have selected a model its parameters will be displayed. Any modifications can then be made by clicking on the column 'Value' to edit the values corresponding to the various parameters. Select File/ Save Model to update this file.

You can delete the selected model from the library by selecting Edit/ Delete.

Extracting Models from an Existing SPICE Netlist

Select File/ Extract from Netlist. From the Open Netlist File window select a file (.cir) and click the OPEN button to open the existing SPICE netlist file.

Once a file has been selected a list of .MODEL lines, from the SPICE netlist file, are displayed. Click on a line to select it.

On selection, the parameters of the selected model will be displayed in a table. Enter the Model Id and the Comment. Edit the values, if required, for the various parameters by clicking on the column 'Value' to get the edit box. After setting the parameters, save the model to an existing model parameter library or to a new library.

EDSpice Simulation References are assigned to parts and not to symbols.

List Generator

List Generator is a utility that allows generating a list containing requisite details of component, Nets, library and Project. A general property description of the objects used in the project may be obtained for easy documentation and future verification. Details of objects specific to a particular circuit design; Layout, Nets, etc are given separately.

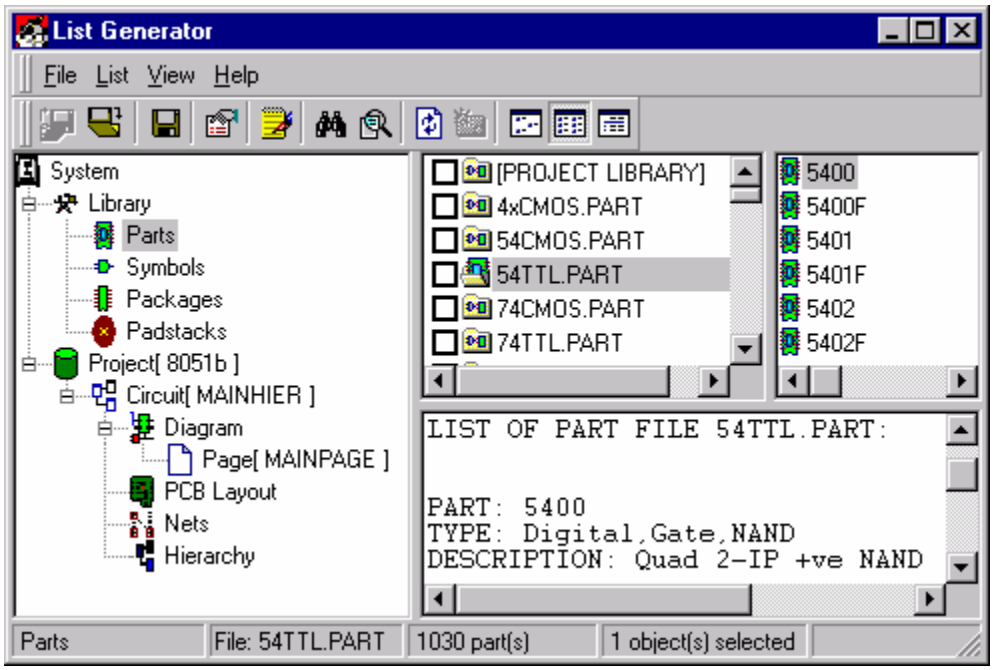


Fig: 2.29 List Generator

Starting List generator

Click System in the project explorer and select one of the following methods.

- Select ***List Generator*** from the task list or task toolbar.
- Select ***List Generator*** from the floating menu that appears on right clicking System.

List Generator appears as shown in Fig .2.29.

File

Open ListBook: Select this option either from the File menu or from the list generator toolbar to open a new window List Book. It displays all the lists saved in the list book using the option Send to ListBook. Open ListBook option will be activated only if there are any entries in the ListBook. ListBook entries will be lost once the List generator is closed. The lists may be saved as *.txt files by selecting the Save List option.

Send to ListBook: Allows to store temporarily the generated list. Select this option either from File menu or from the List generator toolbar to popup a text box. A default name for the list will be provided in the textbox. Click accept to generate a list in that name or type in a new name for the list in the text filed.

Write to DiskFile: Allows to save the generated List as a text file. Select this option either from the File menu or from the main tool bar. Save dialogs box pops up, in which the required name may be entered for saving the List.

Set Library path*:* Allows to set the path for the Library elements.

List

Properties: Displays the property window of the selected item in List Generator.

Generate List: By selecting this option either from the List menu or from the List Generator toolbar, property list of the selected item is displayed. For generating List of the selected item Drag and Drop operation may also be used.

Find: Allows searching a specific library element in the selected library group.

Find Next: Allows searching library elements in part/ symbol/ package/ padstack libraries. If the same element is present in more than one library, the search will stop at the first library. For generating the list of that element, select Generate List from the right click menu/Function toolbar or press F5. For continuing the search to other libraries also press F3 or select from the main menu List/Find next.

Search all libraries: Selecting this search option pops up a search criteria box which extends the search to the entire Library group (for e.g. searches the whole *.PART library for finding a part), for the checked library group or for unchecked library group. If the elements with the same name exist in different Library group, all of them will be included in the list.

Refresh: This option refreshes the displayed list.

Insert Format: This menu is used in conjunction with Generated list menu. Generate list menu allows to list the details of the selected object, but if Insert format menu is also enabled, the list is generated according to the format.

View

The menu items in View when selected/ deselected toggles ON/ OFF the display of the corresponding feature on the workspace.

Tool bar: This option switches ON/OFF the display of toolbar in the list generator window.

Small icon: Allows to set the mode of display of Library elements listed in the explorer window of List generator. This menu item is similar to the standard windows explorer option.

List: Allows setting the mode of display of Library elements listed in the explorer window of List generator. All the library elements may be viewed as a list. This menu item is similar to the standard windows explorer option.

Details: Allows setting the mode of display of Library elements listed in the explorer window of List generator. This menu item is similar to the standard windows explorer option. View/Options menu item allows setting the details to be displayed in the explorer view.

Options: Select this option to pop up a window showing the display settings of Part/Symbol/Package/Padstack items. The selected properties may be viewed by enabling the View/ Details option.

File viewer

This utility allows viewing and editing the files generated from various modules of the package. The file is opened in text/ASCII format. Basic Edit operations such as cut, copy, paste etc. may be performed on the file contents. In addition, text may be searched for and replaced as and if required.

Number of files may be opened at the same time using this viewer. Multiple windows are seen cascaded over one another, by default. Arrangement of windows may be changed by selecting the appropriate option from the window menu.

A new text file may be opened and contents from other files may be inserted into it. It may be saved either as Untitled.txt, by default, or a suitable filename may be assigned to it.

Results of operations such as Gerber artwork generation (Fabrication manager), RAW files (EDSpice) etc. can be viewed in the File Viewer.

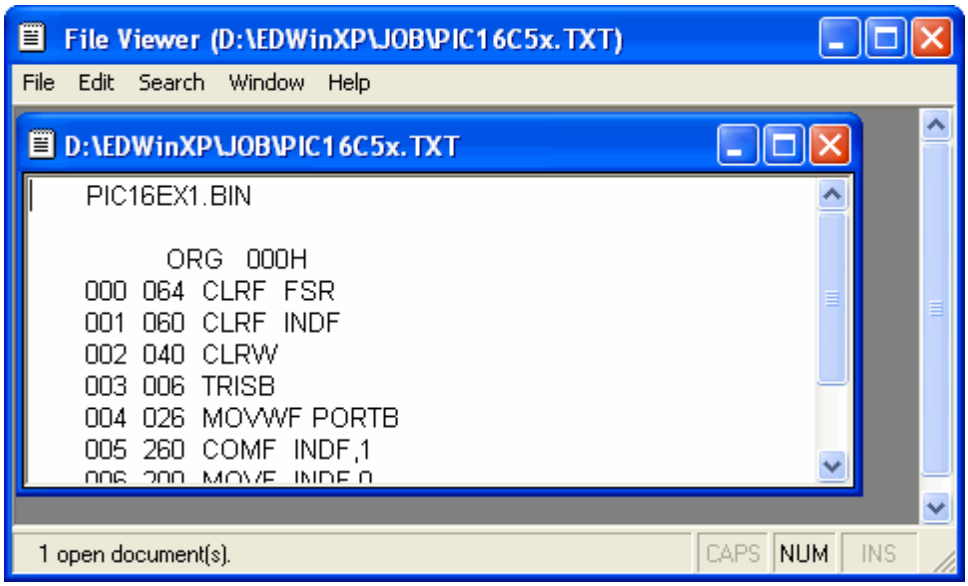


Fig: 2.30 File Viewer

Waveform Viewer

Waveform Viewer may be used to view results in the form of diagram for Mixed Mode Simulator, EDSpice Simulator and Signal Integrity Simulation. This diagram represents the data generated by simulators to present the simulation results in a graphical format. The graphical format may be displayed on the screen, output to a printer or save it as a part to place it on your actual schematic drawing.

In the Waveform Viewer there is no limit to the number of variables that may be loaded. At the same time it is capable of handling any number of samples and hence the simulation time has no limit. The diagrams may be saved to or loaded from a project. Several diagrams can be tiled together to view on a single screen. Tools have been made available to allow users to change the presentation style of the diagram with ease.

Starting Waveform Viewer

This module may be invoked from Project Explorer in the following ways:

- Right click System and select ***Waveform Viewer*** from the list.
- Select Waveform ***Viewer*** from the Task list or from the Task toolbar.

By default, the task toolbar will not be displayed. It may be enabled from View menu in the Project Explorer. The Waveform viewer generates files as a result of simulation done by Mixed Mode Simulator, EDSpice Simulator and Signal Integrity Simulator. The waveform viewer is shown in figure below.

File

Open: Opens an existing data file (*.MCR file) and display it. Selecting this option opens a window. Select the required file and click the **OPEN** button to view the file. You may also Drag and Drop the MCR files from the windows explorer to Waveform Viewer.

Open from Project: Opens the data file already saved to the project***.*** Selecting this option opens a window 'Open Waveforms from Project:' where the lists of the saved files are provided. Check the required files and click the **OPEN** button to view the file. The files may be deleted using the **DELETE** button.

Save: Save the data files to the specified directory. On selecting this option a window opens to specify the file name. Click **SAVE** button to save the file. By default, it stores all data files under \Job with a specified name.

Save All: Save multiple waveforms simultaneously to the specified directory. On selecting this option all waveforms get saved to the specified directory. The waveforms are identified by default names which include the date and time of creation***.***

Save to Project: This option is used to save the currently active waveform to the project. On selecting this option a window 'Save to Project' opens to specify the file name. Click **SAVE** button to save the file.

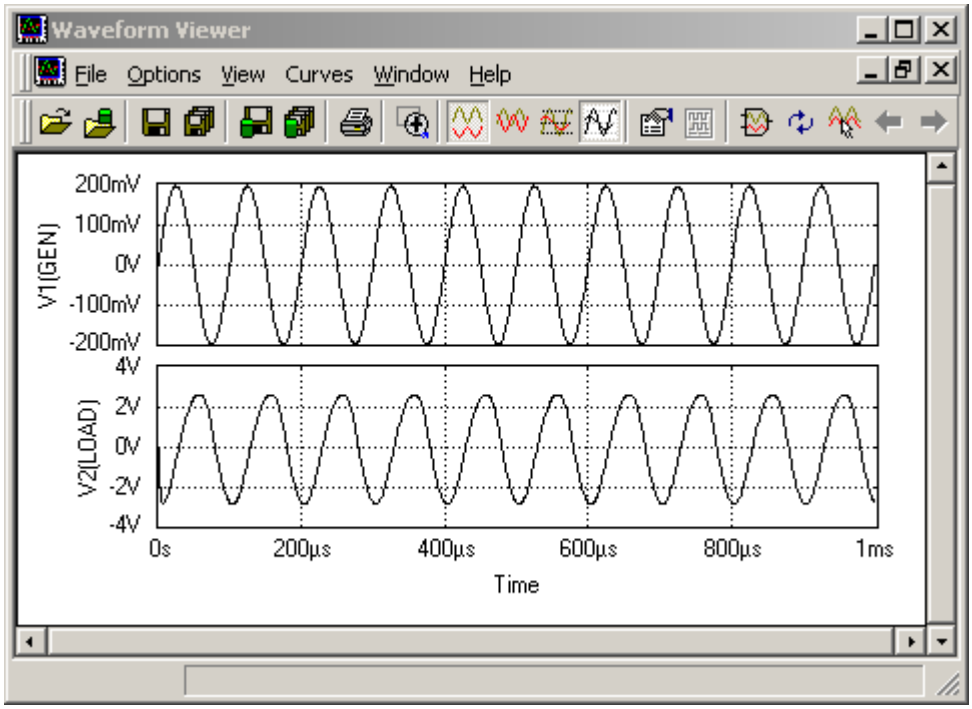


Fig: 2.31 Waveform Viewer

Save All to Project: This option is used to save multiple waveforms simultaneously to the project. On selecting this option all waveforms get saved to the specified directory. The waveforms are identified by default names which include the date and time of creation.

Print: Opens a window "Print" that allows setting the printer and printing options. This window is compatible to that of any windows program. This is used to define the printer setup parameters for printing the waveform. It uses standard Windows routines. Opens a window that allows setting the printer and printing options. Various printer options such as name of the printer, paper size, paper source, number of copies etc. may be entered here.

Copy to Clipboard: Copies the current screen to Clipboard.

Options

The following menu item allows to perform various operations on the waveform variables.

Waveform

Opens a window **"Edit Curves"** that allows to set the variable parameters, waveform appearance and colors for the display of waveforms.

Add / Edit Curves: Add/ Edit Curves tab is used to edit/ add a variable and set its parameters. Select the option buttons 'Edit Curve' or 'Add Curve', as per the requirement. In case of the former, select the curve that is to be edited from the dropdown 'Select curve'. The selected curve will be displayed in the expression box and the curve name is non-editable. In case of the latter, click to **ADD NEW**

CURVES add new curves and give a name to the new curve. The operation that is explained below is the same for both editing curves and adding new curves. Given below is a brief description of the parameters provided in the Fig.2.31.

Add / Edit Curve:	Check either of the checkboxes depending on the operation to be performed. If Add Curves is selected, the DELETE CURVE, MOVE TO LAST, RECALC and APPLY buttons will be displayed.
Select Curve	Select the required curve from the drop down list.
Curve Name	Displays the name of the curve depending on the one selected.
Units	Displays the unit of measurement of the curve. An appropriate unit may be entered in the text-input box.
Expression	It is the expression defined for the variable. The curve for this variable will display the outcome of this

expression. To form the expression, select a variable from the drop down list Argument Variable. Select the function from the drop down list 'Function'. Click **RECALCULATE** and **APPLY** to view the Diagram for the new variable.

Function Lists various functions and basic mathematical operators. Select each one, as desired. The function gets displayed in the Expression frame. As more functions are selected, the expression size increases.

Argument variable Lists the argument variables available for the project.

Scaling/ display Mode Enable either of the checkboxes to set the scaling mode to Linear or Logarithmic. The logarithmic mode is restricted to cases when the values of Minimum and Maximum are both greater than zero

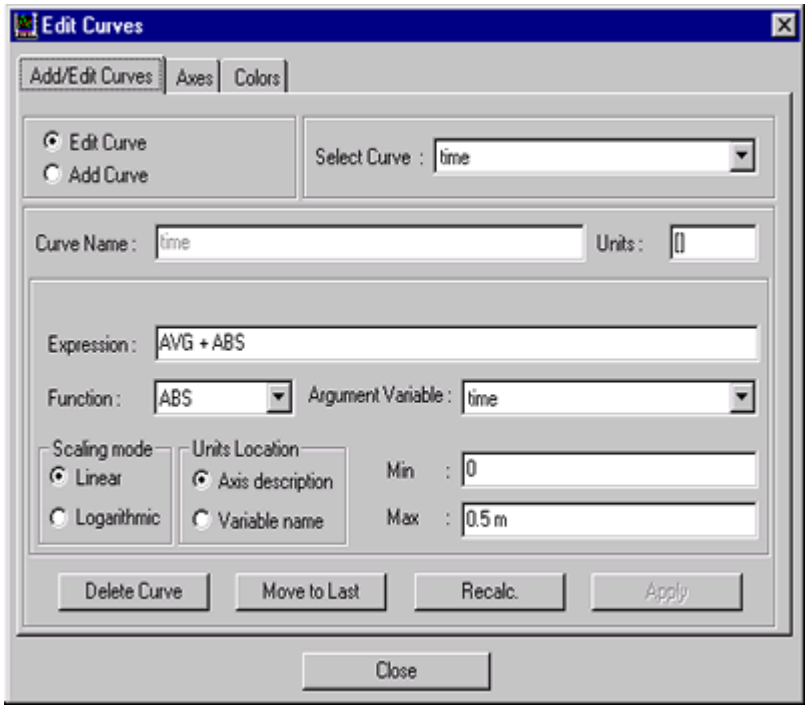


Fig: 2.32 Add/Edit Curves

Units Location Location of units on the diagram may be chosen at axis or after the first variable name. Enable either one of the checkboxes as desired.

Min, Max Set the minimum and maximum range for the selected variable. The curve will be displayed only for that range.

Delete Curve Deletes the present curve

Move to Last Permits movement of the selected variable to the last position.

Recalculate Use this button together with **APPLY** button to view the Diagram for the new variable, after expression and parameters have been set.

Apply Use this button **RECALCULATE** together with button to view the Diagram for the new variable, after expression and parameters have been set.

Example

Suppose a new curve (crv2) is to be defined. Let V (GEN) and V (LOAD) be the existing variables. Let the new curve (crv2) represent the output of the expression V (GEN) + V (LOAD). Define the expression by selecting the variables [V (GEN),

V (LOAD)] from the drop down list Argument variable and the function '+'. from the drop down list 'Function'. Click **RECALCULATE** and **APPLY** to view the Diagram for the new variable.

Axes: Axes tab allows to set certain parameters to mandate the Waveform appearance. From this tab, the user may mandate over the waveform appearance.

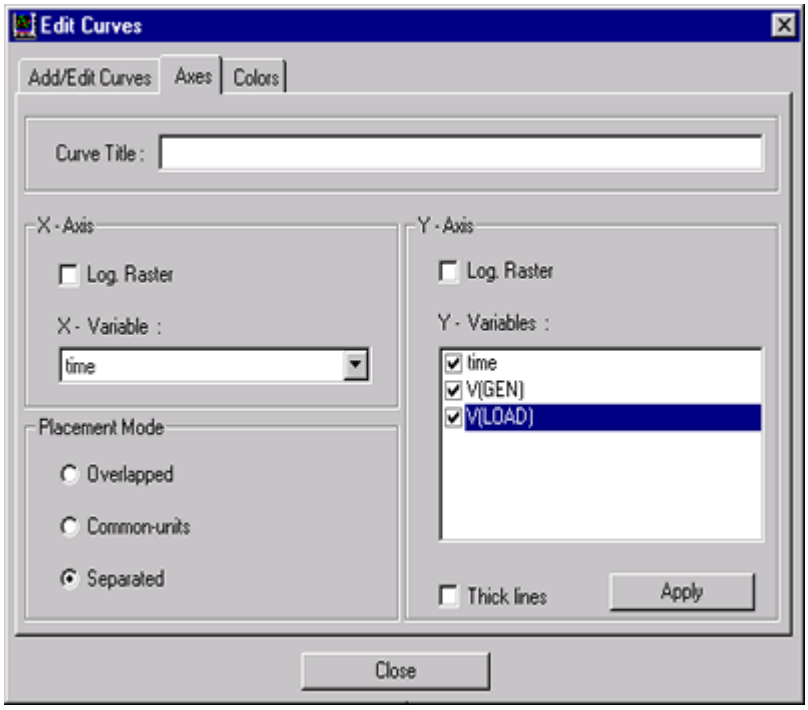


Fig: 2.33 Axes

The following controls are available:

X-axis frame box: The Log. Raster check box enables the logarithmic diagram rastering, when the X-variable is displayed using the logarithmic scaling mode. A drop-down list box displays current X-variables and allows selecting the X-variable from the available ones. By default it is the first one.

Y-axis frame box: The Log. Raster check box enables the logarithmic diagram rastering, when any of the Y-variable is displayed using the logarithmic scaling mode. The waveform that is to be displayed on the Y-Axis may be checked here.

The user may specify up to 8 variables to display 8 curves. The Thick lines check box enables the double-width curve drawing (for all curves).

May be viewed only for analog circuits.

Option buttons are grouped in the Placement mode frame box. Select one of the three curve placement modes.

Overlapped: Changes the curve placement mode to Overlapped. All curves are placed in one frame and scaled independently to obtain maximum amplitude. Each curve has separated Y-axis description.

Common-units Usually the curve of each variable is displayed in a sub frame. Each sub-frame has its own Y-axis description. The waveform frame is thus divided into sub-frames. On selecting this option, curves with the same units are placed into the same waveform sub-frame and scaled commonly.

Thick Lines Enable this checkbox to view the waveforms as thick lines.

Apply Saves the changes and enforces them immediately.

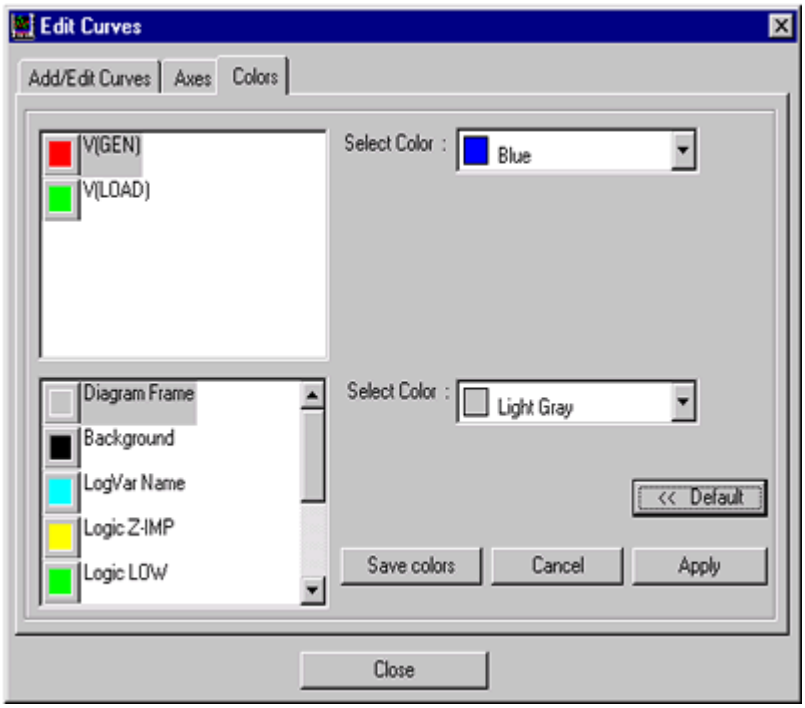


Fig: 2.34 Color

Color: Colors tab allows to set the colors for presenting the waveform. This tab allows to select colors for the waveform components and also to set the background color. The colors assigned to all waveform components are displayed in two widows. To assign a new color to a waveform component, select the desired waveform component from the window and select the color of your choice from the dropdown. Clicking the DEFAULT button assigns the default colors to the waveform components.

Clicking the CANCEL button cancels any color assignment made. The SAVE COLOR button saves the color setting made even after exiting.

Logic Analyzer

Opens a window "Word Format Output" that allows to analyze the logic state of the test points placed on the schematic circuit. The word size may be represented in 8 bit, 16 bit, and 32 bit and the values may be in decimal, binary, hexadecimal or octadecimal code according to the selection made.

Given below is a brief description of the parameters provided in the "Word Format Output" window.

Word size This option automatically gets set, according to the test points placed on the schematic circuit. The test points on the Y-axis in the diagram will be listed in the first list box. The bits will be displayed in the second list box according to the selected word size. Any bit may be assigned to any test point. Select a bit and double click the test point parameter in the fist list box to place the parameter against the selected bit or click >>. In the same way to remove the parameter after placing, double click the required parameter or click <<.

Example: Test points placed is 14 in number, then word size gets set to 16, if it is 5 then word size would be 8. The word size gets set to the nearest higher value available.

Recalculate Allows viewing the values of the result in the third list box. These values will be represented according to the code selection (binary, decimal, octadecimal or hexadecimal code). The result thus displayed in bits allows verifying the time of rise up and rise down of the particular test points placed against the selected bit.

Save File As The Result may be saved as *.DGS (Digital source output) file and PWL (Piecewise linear source output to feed as input to Spice). This may be done by selecting the menu items Digital source output or PWL source output.

Create Special Part

This option is used convert the waveform as a Part to be loaded into the schematic diagram. The Create Special Part menu option allows saving the currently displayed waveform as a part to the project. The user can define the name of the part and use the part for loading to the Schematic Editor from the project library. This part (waveform) may be used on the schematic to point out the output/ input wave at various points of the circuit. On selecting this option, a window pops up which allows entering the name to be assigned to the Part. The part may be saved to the disk library from Library Explorer module.

 *Open the Project Library in Library Explorer and copy the part. Paste it to a new part library or user created library, since the system does not allow to alter its own library contents.*

View

Separated Allows viewing each curve in a separate sub frame and may be scaled independently to obtain maximum amplitude. Each curve has its own separated Y-axis description. This option is usually required once the Overlapped option has been activated.

Common Units Usually the curve of each variable is displayed in a sub frame. Each sub-frame has its own Y-axis description. The waveform frame is thus divided into sub-frames. On selecting this option, curves with the same units are placed into the same waveform sub-frame and scaled commonly.

Overlapped Changes the curve placement mode to Overlapped. All curves are placed in one frame and scaled independently to obtain maximum amplitude. Each curve has separated Y-axis description.

Monochrome Allows to toggle the waveform color between Monochrome and color.

Reset Retains the diagram after any zooming operation has been performed on it.

Curves

Allows to select the curves for display. Selecting this menu item opens a window where all the curves that are generated as a result of the analysis are listed. Check the required curves for display and click the DISPLAY button. Only eight curves may be displayed at a time. Tools are provided in the toolbar to display the next set of eight curves in the list. Select  or  to display previous or next set of curves.

Windows

Cascaded Allows to arrange all the currently open waveforms one above the other.

Tile Horizontally Allows to arrange all the currently open waveforms horizontally on the screen.

Tile Vertically Allows to arrange all the currently open waveforms vertically on the screen.

Arrange Icons Arranges the icons of minimized waveforms.

Close All This menu option allows to close all the waveform windows of the Waveform Viewer

How to use Waveform viewer?

The Waveform viewer generates files as a result of simulation done by Mixed Mode Simulator, EDSpice Simulator and Signal Integrity Simulator.

Change diagram's appearance

The Waveform viewer analyzes all input data and does all the scaling before making a new diagram. However, the settings can be changed to the requirements with the help of Waveform pull down menu of Options.

Diagram menu commands globally used are:

- Select the independent X-variable.
- Select another set of Y-variables to display.
- Choose between linear and logarithmic raster of the diagram frame.
- Add a diagram title text.
- Choose one of three curve placement modes.

Select single or double width of diagram curves (The Thick lines check box enables the double-width curve drawing) for all curves.

May be viewed only for analog circuits.

Assign colors to the diagram frame; diagram curves and background with the help of *Options/ Waveform/ Colors* from the menu.

Set each variable individually from *Options/ Waveform:*

Choose linear or logarithmic scaling mode for X- and Y-variables.

Set scaling range (min/ max value) for X- and Y-variables.

Change names and units of variables.

Add new variables using arithmetic expressions.

The finally drawn diagram may be copied to the Windows Clipboard as a bitmap or saved as a part in the library.

How to add new curves?

The user can add new diagram variables based on the existing ones. For example: We will create a new variable named Mean that is equal to the arithmetic mean of the variables VarA and VarB:

- Choose the Options/ Waveform / Add/Edit tab.

- Type in the new variable name and eventual units.
- Enter the following expression: (VarA+VarB)/ 2
- Press the RECALC push-button to generate the new variable samples

Expressions Syntax

Constants: They are the standard floating-point numbers and they may use the scale suffixes from "p" (Pico) till "G" (giga). Units used in constants are ignored.

Operators: They may have one or two arguments. Available arithmetic operators are (in the order of precedence)

- ( ) parenthesis
- ^ exponentiation
- - negation
- * / multiplication, division
- + - addition, subtraction

Functions:

They have the highest priority. Available functions of expressions x, y is:

ABS(x)	|x|
CABS(x,y)	sqrt(x²+y²)
SGN(x)	sign of x: { -1,0,+1 }
INT(x)	max. integer less or equal x
DB(x)	20·log10(|x|)
EXP(x)	e^x
PWR(x,y)	|x|^y
LOG(x)	log base e
LOG10(x)	log base 10
SQRT(x)	square root of x
SIN(x)	sin of x radians
COS(x)	cos of x radians
TAN(x)	tan of x radians
ATAN(x)	Arc tan of x, returns range ± ?/2 rad
ATAN(x,y)	Arc tan of x/y, returns range ±? rad
D(x)	derivative of x respect to the sampling domain: (dx)
D(y)/D(x)	derivative of y respect to the x: (dy/dx)
S(y ,D(x))	integral of y over the x, with the step D(x): (òy·dx)
S(y)	integral of y over the sampling domain, assuming dx=1

Waveform viewer Other functions

MIN (variable)	minimum value of variable samples
MAX (variable)	maximum value of variable samples
AVG (variable)	average value of variable samples: å(x)/N

RMS (variable)	RMS average value of variable samples: sqrt (å(x²)/N)
SAMPLE	current sample number, from 0 to N-1

There are number of pre-defined constants in nutmeg. They are:

- pi (3.14159...)
- plank Planks constants (h=6.626200e)
- Kelvin Absolute 0 in Centigrade(-273.15 deg C)
- boltz Bolltzman's constant(1.3806226e-23)
- echarge The charge on an electron(1.6021918e-19C)
- i Square root of -1
- c Speed of light(299,792,500 m/sec)
- e The base of natural logarithms (2.71828...)

They are all in MKS units. If there is another variable that conflicts with one of these names then it takes precedence.

How to obtain Lissajous Pattern?

Lissajous pattern is produced when two Voltages with different Frequency and Phase are applied simultaneously to the X & Y coordinates. The type of pattern observed depends upon the ratio of Frequency and also upon the relative phase of the two waves. With the help of Lissajous patterns the unknown frequency and phase angle may be measured.

Waveform Viewer allows generating Lissajous patterns for the unknown frequency measurement in the following way. After desired analysis, select Option | Waveform from the Waveform viewer main menu. An Edit Curves window pops up from where select Axes tab. Set the X and Y variables. Thus Waveform viewer generates diagram with different shapes which may be obtained by varying the frequency and phase angle of one source.

MM Simulation Model Generator

MM Simulation Model Generator enables to generate models of digital and analog circuit elements. This tool serves the purpose of making simulation much faster .For creating models of digital elements, generator processes logic function defined in VHDL or in the form of truth table. The function of analog elements may be very precisely described in SPICE netlist format. Therefore the source for analog model generation is ASCII file containing SPICE sub-circuit.

EDPrimX is a tool which can be used for creating both analog and digital models, however it assumes programming knowledge and the user has to build his own simulation primitive dll.

Starting MM Simulation Model Generator

- Select MMSimulation ***Model Generator*** from the task list or task toolbar of Project Explorer.

- Select ***MMSimulation Model Generator*** from the floating menu that appears on right clicking System.

A window titled Model Generator for Mixed Mode Simulator appears as shown in Fig.2.35.

For Digital Model Project

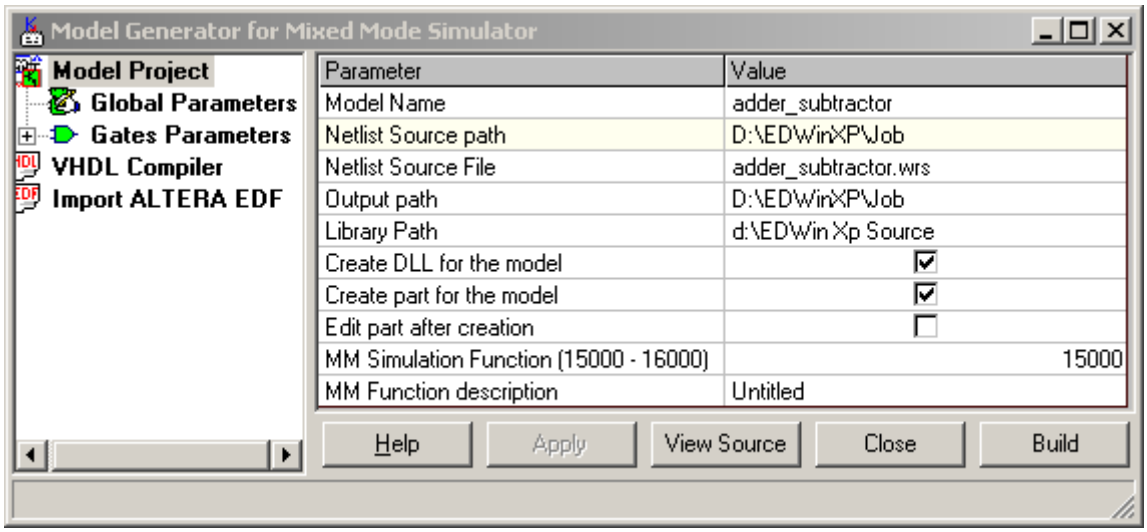


Fig: 2.35 Model Generator for Mixed Mode Simulator

Operation: Select Digital model type from Select Model Type. Double click on the cell next to VHDL Source File name to select the file. As soon as the file is selected, MM Generator will compile the VHDL file and exhibit the results in File Viewer window.

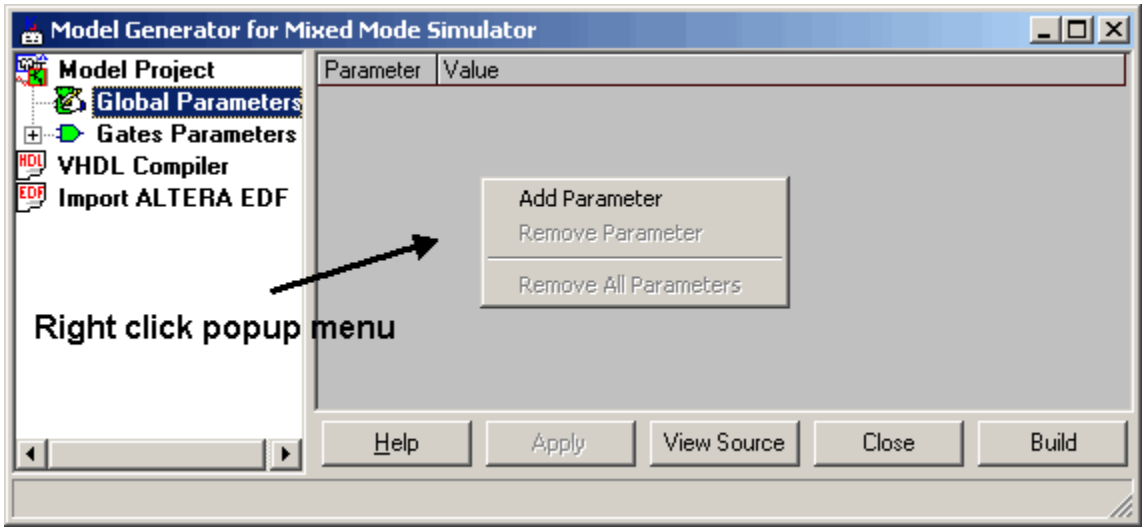


Fig: 2.36 Adding Parameters

The errors in the VHDL file (if any) have to be corrected before proceeding. Once the VHDL file is error free, the focus automatically moves to the **Model Project** window.

Enter the **Global Parameters** by Clicking on Add Parameters as shown in Fig.2.35 When you click on add parameters, Set Global Parameter Window appears as shown in Fig.2.37

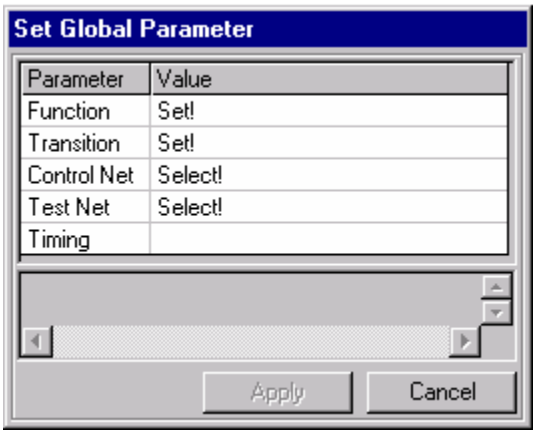


Fig: 2.37 Set Global Parameter

Select a value from the dropdown list for Function, Transition, Control net and Test net, enter a value for Timing and then press Apply. Once parameters are entered, the menu items Remove Parameter and Remove all parameters become active in the Global Parameters window.

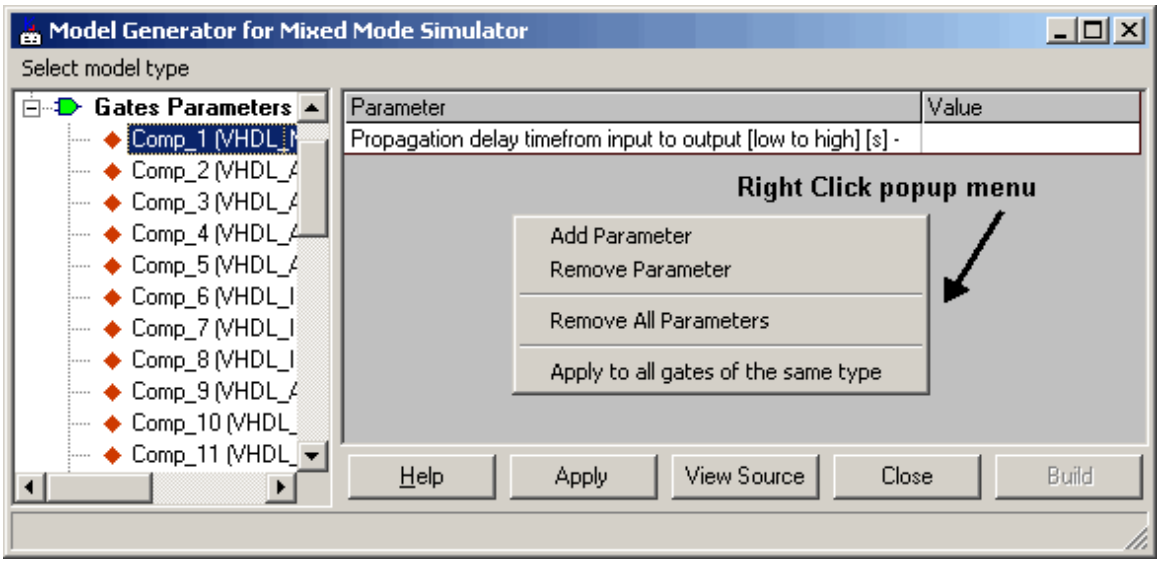


Fig: 2.38 Set Gate Parameters

After the global parameters are set, the **Gate Parameters** may also be set. Once Gate parameters are set, enter the function description and press the Build button to compile the dll. If you would like to make more changes to your model, the Visual

C++ source files contained in the Output Path can be edited. After editing the files, compile the dll and copy it to the \Lib folder.

The window is as shown in Fig.2.38.

For Analog Model Project

The logic function of analog elements may be very precisely described in SPICE netlist format. Therefore the source for analog model generation is ASCII file containing SPICE sub-circuit.

The generation process is automatically performed in two stages:

- Conversion of source sub-circuit into C language project of MM simulation model .DLL.
- Compiling, linking and storing of model .DLL in MM Simulator model library, ready to be assigned to circuit components and used for simulation

Operation: Select Analog model type from Select Model Type. Model Project window for Analog model appears as shown in Fig: 2.38.

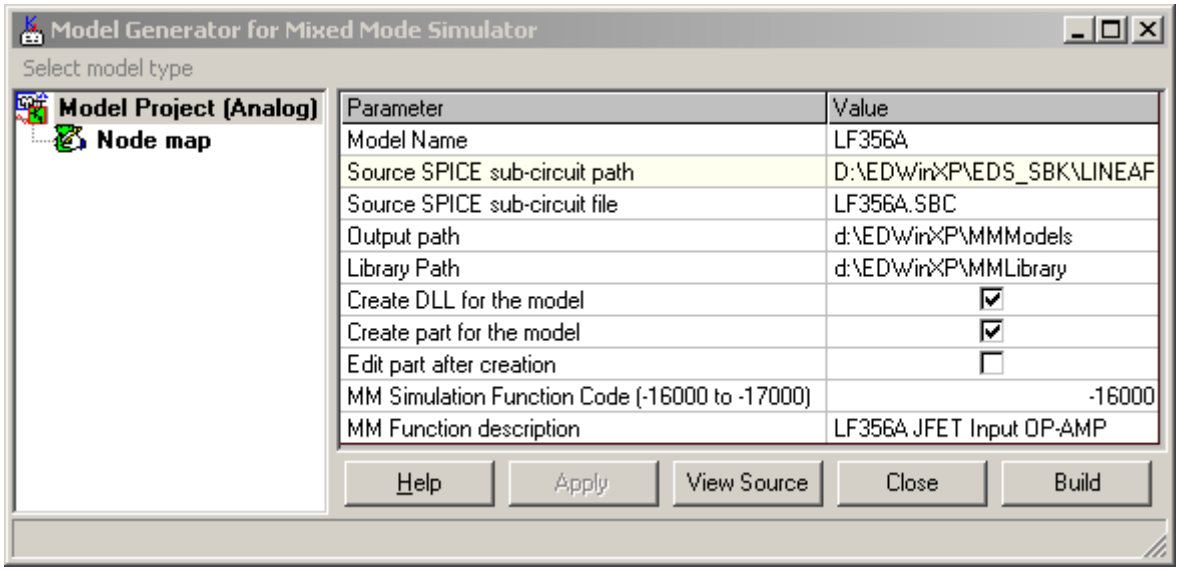


Fig: 2.39 Model Project window for Analog model

Browse to select the source SPICE sub-circuit file.

Once the source file is selected, entry simulation names are generated using node names from the sub-circuit.

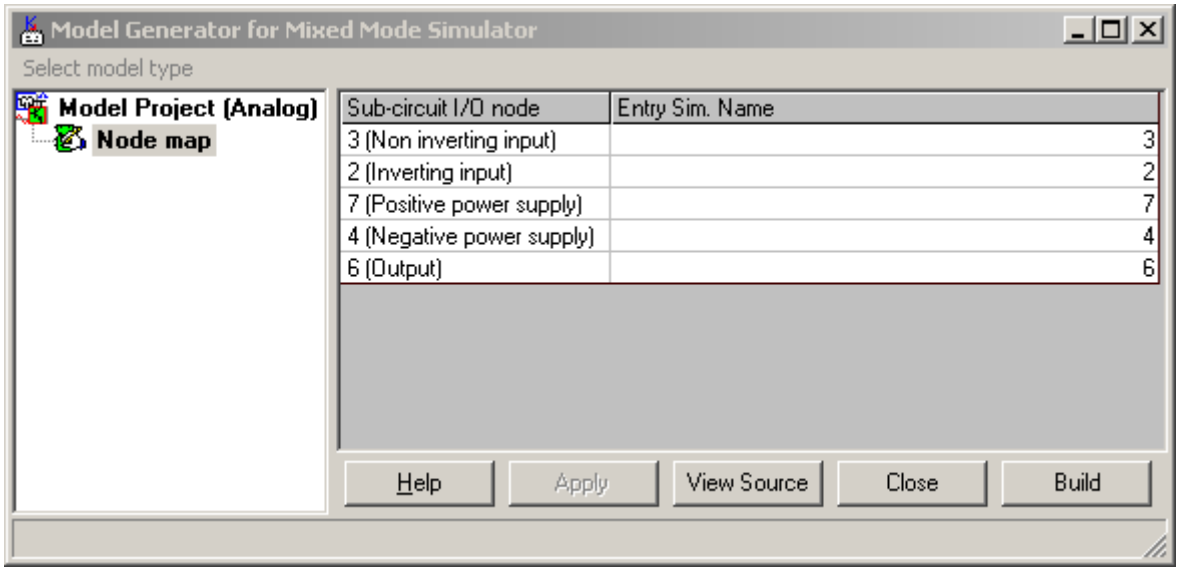


Fig: 2.40 Node Map

Each I/O Nodes for feeding signals to/from models have to be assigned names that must be unique within given model. These names must be identical with simulation entry names in the graphic symbol of circuit element (part) to be simulated by model. For example the line .SUBCKT OPAM 1 2 3 will produce entry simulation names "1", "2" and "3". Numbers explain poorly the function of each node and in the dialog Node map users may specify more meaningful names.

Click on Build button Click on Build button MM Generator will compile the subcircuit file and exhibit the results in File Viewer window.

VHDL Compiler

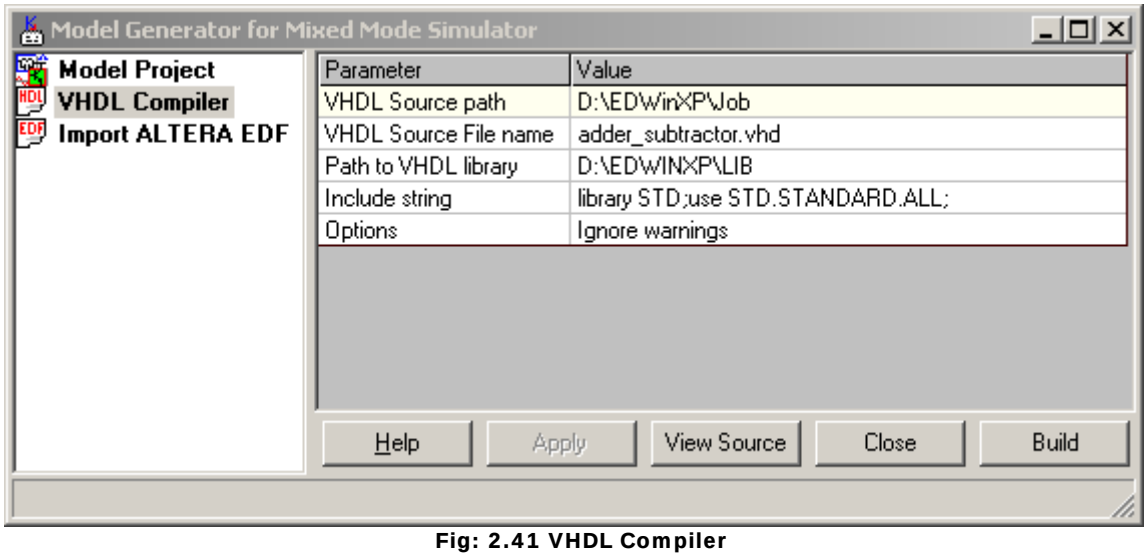


Fig: 2.41 VHDL Compiler

Browse to select VHDL Source File name. As soon as the file is selected, MM Generator will compile the VHDL file and exhibit the results in File Viewer window.

The errors in the VHDL file (if any) have to be corrected before proceeding. Once the VHDL file is error free, the focus automatically moves to the Model Project window.

Import ALTERA EDF

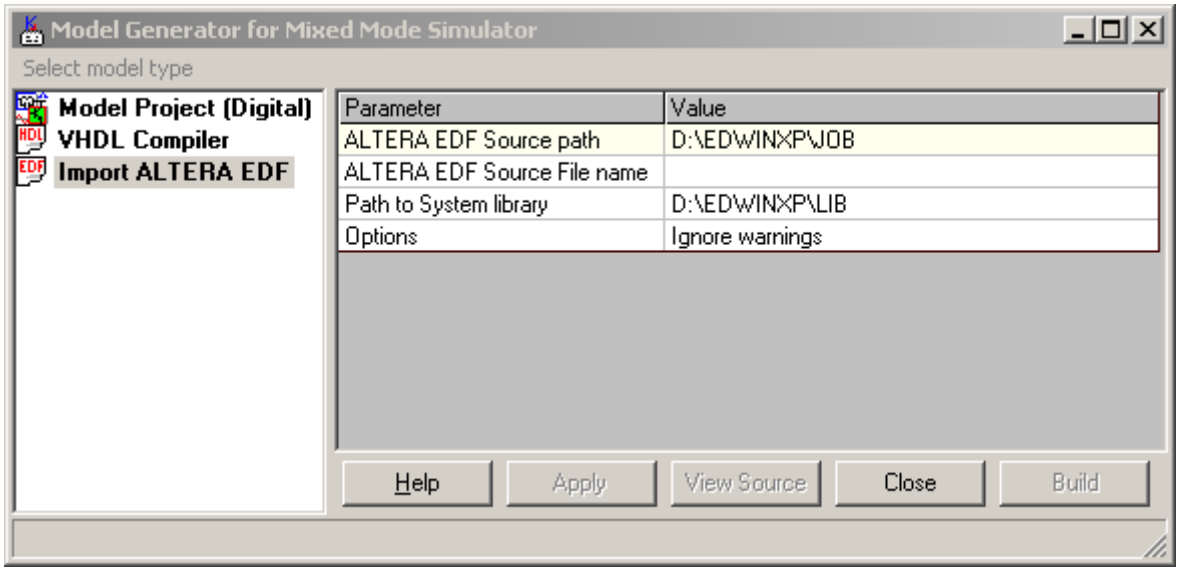


Fig: 2.42 Import ALTERA EDF

To import ALTERA EDF

Browse to select the Source File. As soon as the file is selected, MM Generator will compile the ALTERA EDF file and exhibit the results in File Viewer window.

The errors in the ALTERA EDF file (if any) have to be corrected before proceeding. Once the file is error free, the focus automatically moves to the Model Project window.

EDSpice Simulation Model Generator

This tool converts a VHDL source file to a simulatable component in EDSpice, the SPICE based simulator (which is a plug-in). This also serves the purpose of making simulation much faster.

Since VHDL can only be used to create digital models, only digital simulation models can be created using EDSpice Simulation Model Generator. Earlier, knowledge of programming was essential for writing digital models. It would be much easier for an electronic engineer to create the models using VHDL rather than learn other non-standard programming languages for creating models. Therefore a need for developing a tool arose which could convert VHDL models to SPICE models.

EDComX is a tool which can be used for creating both analog and digital models, however it assumes programming knowledge and the user has to build his own simulation SPICE Model.

Starting EDSpice Simulation Model Generator

- Select ***EDSpice Simulation Model Generator*** from the task list or task toolbar of the Project Explorer.
- Select ***EDSpice Simulation Model Generator*** from the floating menu that appears on right clicking System menu in Project Explorer.

A window titled Model Generator for EDSpice Simulator appears as shown in Fig.2.43.

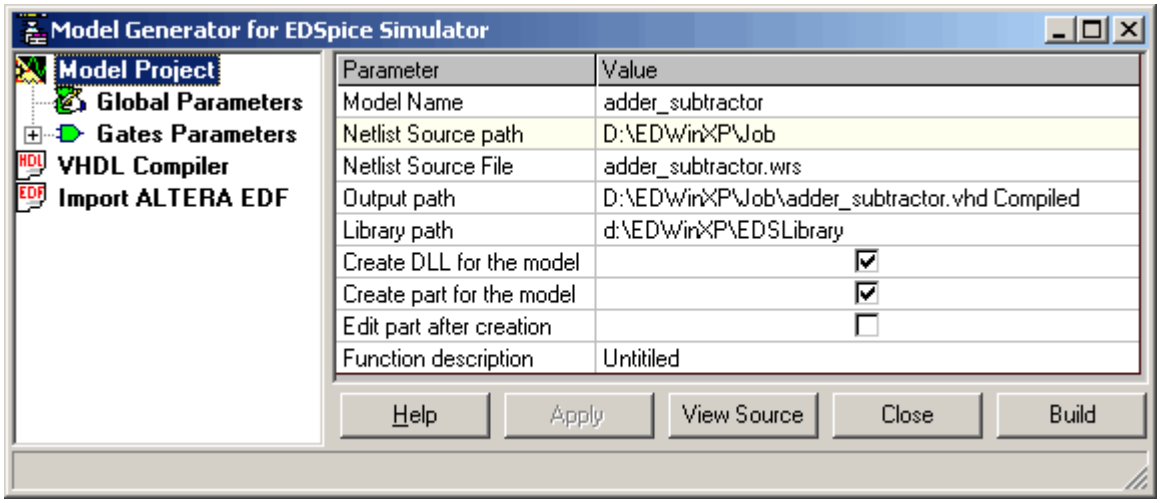


Fig: 2.43 Model Generator for EDSpice Simulator

Browse to select VHDL Source File name. As soon as the file is selected, EDSpice Generator will compile the VHDL file and exhibit the results in File Viewer windows.

The errors in the VHDL file (if any) have to be corrected before proceeding. Once the VHDL file is error free, the focus automatically moves to the Model Project window.

Now values of Global Parameters can be entered by right clicking and add parameters in the Set Global Parameters pop up as shown in Fig.2.44.

Select a value from the dropdown list for Function, Transition, Control net and Test net, enter a value for Timing and then press Apply.

Once parameters are entered, the menu items Remove Parameter and Remove all parameters become active in the Global Parameters window.

Once the global parameters are set, the parameters for the individual gates may also be set.

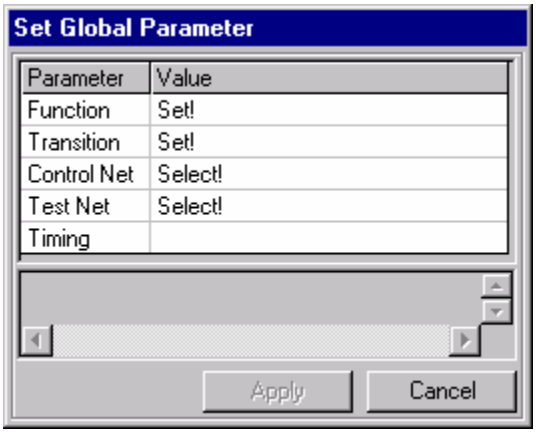


Fig: 2.44 Global Parameters for EDSpice Simulator

Import ALTERA EDF

To import ALTERA EDF

Browse to select the Source File. As soon as the file is selected, EDSpice Generator will compile the ALTERA EDF file and exhibit the results in File Viewer window.

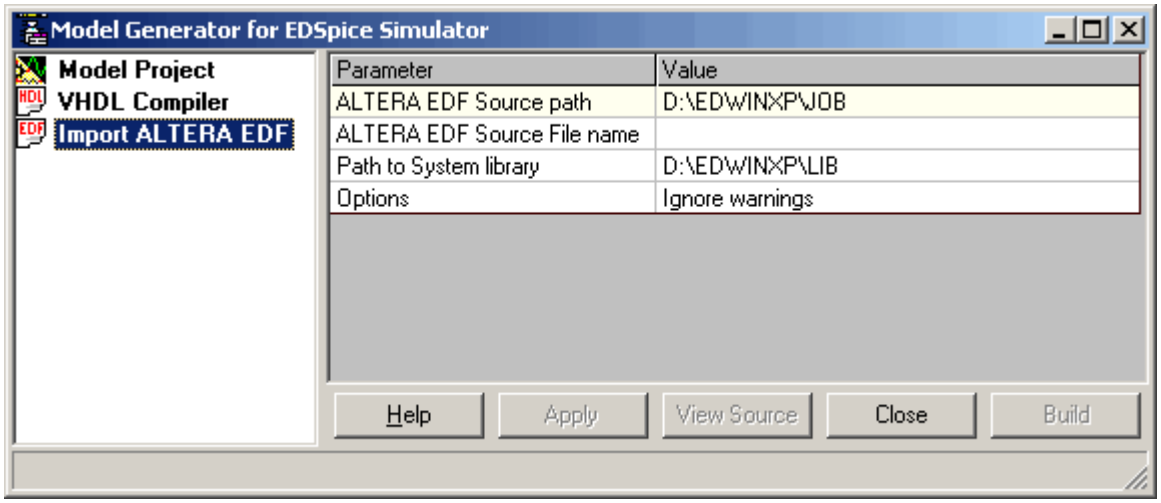


Fig: 2.45 Import +ALTERA EDF for EDSpice Simulation

The errors in the ALTERA EDF file (if any) have to be corrected before proceeding. Once the file is error free, the focus automatically moves to the Model Project window.

VHDL Editor

VHDL Editor is basically an editor for writing VHDL program. Its working is very much similar to any normal programming editor. All keywords present in the source are highlighted in blue. The source code may be compiled and error messages displayed to help quick debugging.

Invoking VHDL Editor

This module may be invoked from Project Explorer in following ways:

- Right click System and select VHDL Editor from the list.
- Select VHDL Editor from the Task list or from the Task toolbar.

The VHDL Editor opens as shown in Fig.2.46.

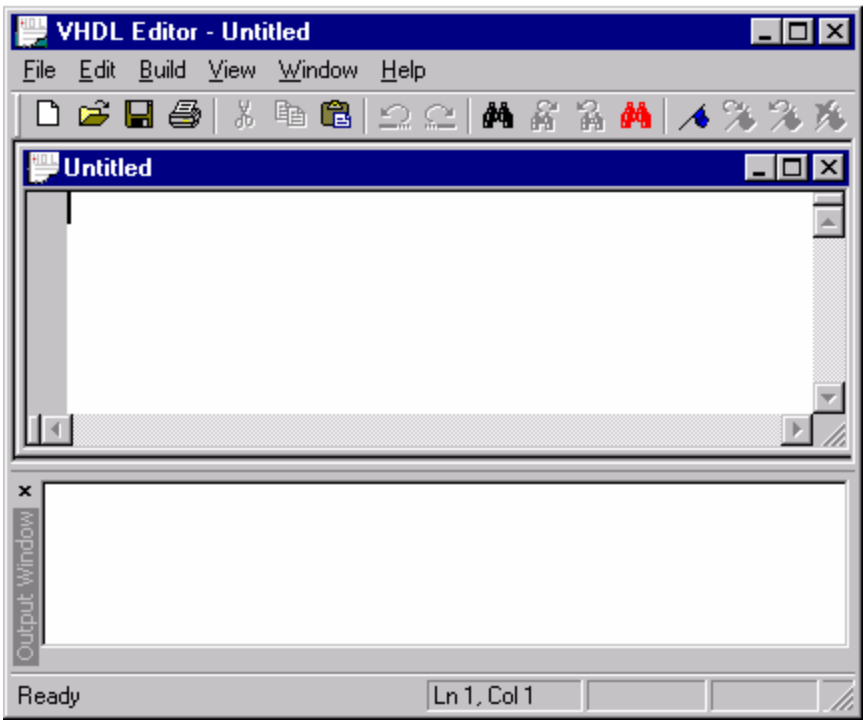


Fig: 2.46 VHDL Editor

Some main features of VHDL Editor are:

- It compiles the source file and generates wirelist (*.wrs) output file.
- The output file (*.wrs) may be imported directly to EDWinXP Schematic Editor.
- Helps to generate simulatable models in Mixed Mode & EDSpice Model Generators.
- Helps to convert the (*.wrs) file to Xilinx, CUPL and JEDEC formats.

The Main menu of the module is given below.

Build

Compile: Compiles the *.vhdl source file and generates the *.wrs file. Enable this menu item from Build menu to compile the VHDL source file and generate wirelist file (*.wrs). Compilation stops at the first occurrence of error and the error message gets displayed in the output window. Double click on the message to highlight the

line within the code. The display of compile errors may be switched off either from the menu *Edit* | *Switch Off Compile Errors* or by double clicking the message in the output window. The output window may be made visible from the menu *View* | *Output.*

COMPILE & IMPORT: Compiles the *.vhdl source file, generates the *.wrs file and imports gate level circuit to the Schematic Editor. Select this option from Build menu. The compiled output file (*.wrs file) gets loaded in Netlist/Wirelist Export & Import dialog (Refer page: 78).

Create MM Model: Opens the Mixed Mode Simulation Model Generator, which helps to generate a simulatable model. Select this menu item from Build menu. The *.vhdl source file is compiled and the output file (*.wrs file) gets loaded in Mixed Mode Simulation Model Generator (Refer Page: 63).

Create EDSpice Model: Opens the EDSpice Simulation Model Generator, which helps to generate a simulatable model in EDSpice. Select this menu item from Build menu. The *.vhdl source file is compiled and the output file (*.wrs file) gets loaded in EDSpice Simulation Model Generator (Refer Page: 68).

Create Xilinx Output: Opens Netlist/Wirelist Export & Import utility to convert the compiled vhdl output file (*.wrs) to Xilinx netlist format (*.edn).Select this menu item from Build menu. The *.vhdl source file is compiled and the output file (*.wrs file) gets loaded in Netlist/Wirelist Export & Import dialog (Refer page: 78).

Create CUPL Output: Opens Netlist/Wirelist Export & Import utility to convert the compiled vhdl output file (*.wrs) to CUPL netlist format (*.pld) .Select this menu item from Build menu. The *.vhdl source file is compiled and the output file (*.wrs file) gets loaded in Netlist/Wirelist Export & Import dialog (Refer page: 78).

Create JEDEC Output: Opens Netlist/Wirelist Export & Import utility to convert the compiled vhdl output file (*.wrs) CUPL netlist and in turn to JEDEC netlist format (*.jed and *.map).Select this menu item from Build menu. The *.vhdl source file is compiled and the output file (*.wrs file) gets loaded in Netlist/Wirelist Export & Import dialog.

View

Toolbar: Toggles on/off the display of toolbar.

Status Bar: Toggles on/off the display of status bar.

Output: Toggles on/off the display of output window.

Window

New Window: Open a new VHDL file.

Cascade: Displays all open windows in cascaded form.

Tile: Tiles all the open windows.

***Arrange Icons*:** When multiple windows are in minimized state, this menu arranges the icons at the bottom of the editor.

Save Settings

This feature allows you to save the particular settings used in the editors & viewers separately in a file.

Operation: Enable Save Settings from Project Explorer/ System. Save Settings File As window appears, browse the path to which file has to be saved. Click on ***save*** button to save your settings.

Restore Settings

This feature allows you to restore the settings used in the editors & viewers back at any time even after un-installation or reinstallation.

Operation: Enable Restore Settings from Project Explorer/ System. Open Settings File window appears. Browse the settings which are to be restored. Click on ***Open*** button to restore your settings.

Library

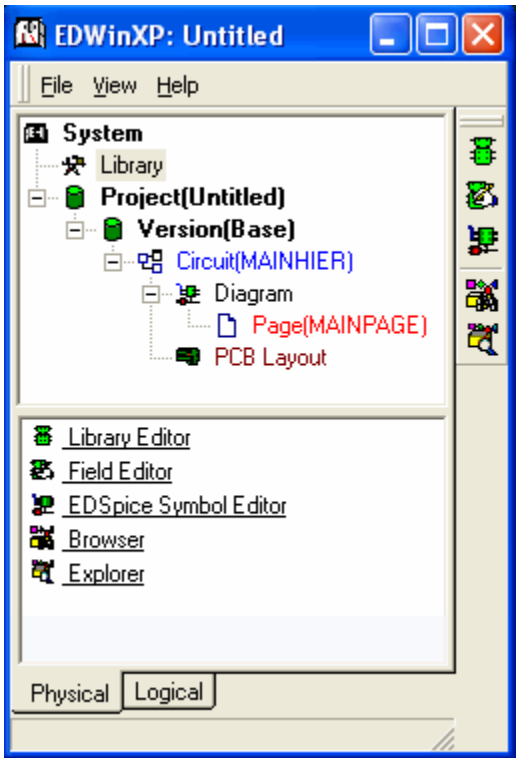


Fig: 2.47

Libraries are the building blocks of any EDA based Electronic Designs and EDWinXP provides a flexible arrangement of its Library elements.

Library structure of EDWinXP can be viewed as described below:

Part Library: Part Library integrates the Schematic and Layout elements of all EDWinXP Libraries. That means one Part Library element includes its symbol used in Schematic Diagram and the Package used in Layout Design

Symbol Library: Symbols are used in any Electronic design solution to represent the graphical form of components such as Semiconductors, Connectors etc. in Schematic Diagrams. Various representations are based up on of widely accepted standards like ANSI, IEC etc.

Package Library: Package is the physical representation of any component such as Semiconductors, Connectors etc. used in the Layout Design of a Printed Circuit Board. A Package thus includes various attributes including pin dimension of the component. Packages are designed in accordance with standards like JEDEC and datasheets of manufactures.

Padstack Library: Padstacks can be treated along with Package and contains the information of different pads for different layers of a PCB.

Project

Allows creating a new project, opening an existing one, load and/or save projects, viewing project properties, adding circuits and setup the options for the project etc.

New Project

Creates a new project by clearing the loaded project.

Open Project

Opens an existing project. Before opening, the system prompts for saving the current project. Also the thermal Information for the parts that could not be updated is listed in dialog window.

Save Project

Saves the currently loaded project.

Save Project as

Saves the currently loaded project to a new name.

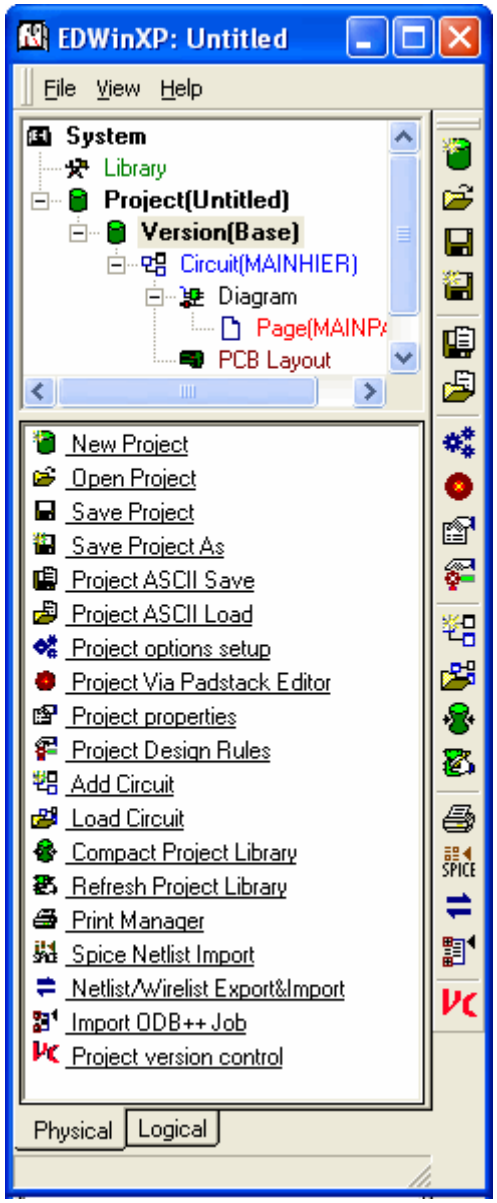


Fig: 2.48

Project ASCII save

Saves the loaded project in an ASCII file format.

Project ASCII load

Loads a project that was saved in ASCII format.

Project options setup

This task enables the user to open Options window where the options may be set which reflects only for the current project.

Project Via Padstack Editor

This utility is used to set default parameters for a selected via padstack on each layer. Refer Default Via Padstack Editor page: 32.

Project properties

Sets the project properties such as designer name, revision and password to the current project design. Also allows to change values of certain entities.

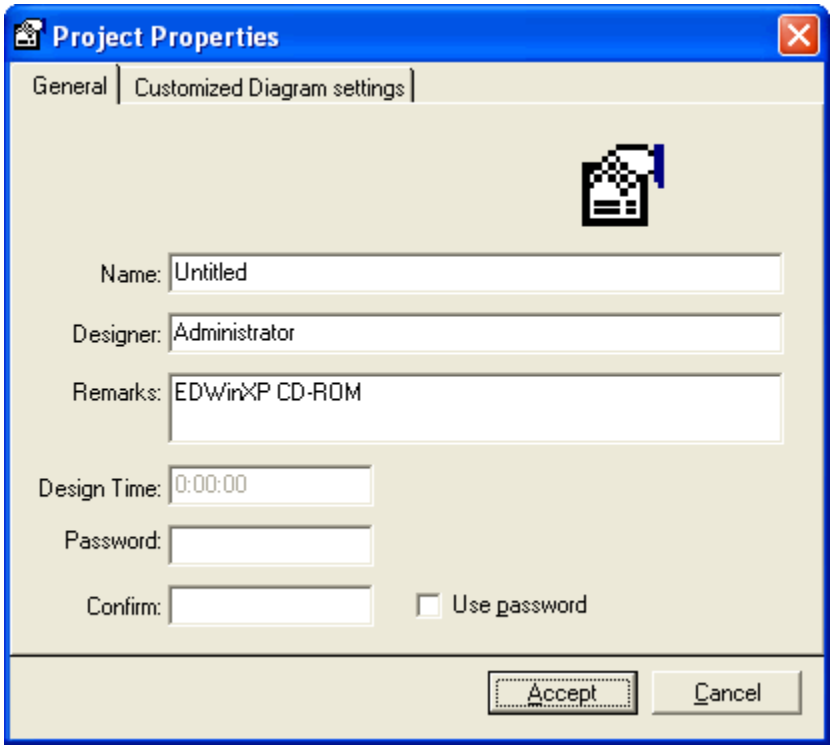


Fig: 2.49

It is necessary to save the project to make the changes to Project properties, effective.

Project Design Rules

Pops up EDWinXP – DRC Setup to set certain default Design Rules to work with EDWinXP. This utility is used to preset certain parameters for manual, semiautomatic and automatic routing of traces and component placement. With the given parameters, the Layout conducts a design rule check and any problems are marked by an Error label. The errors may be queried using the Redraw/ Error. The design rule settings may be saved as a permanent setting or may be set for the circuit or for the current project only. The design rule settings may be saved as a permanent setting or may be set for the circuit or for the current project only.

Add Circuit

To add a circuit to the current project.

Load Circuit

To load an existing circuit and add to the current project.

Compact project library

Deletes all unused symbols, package, padstack and parts from the project library.

Refresh Project Library

Refreshes the symbols, package, padstack and parts in the project library.

Print Manager

Print Manager allows printing the project designs and various files generated from different modules of the program with ease at a single stretch. The set of options provided in this utility makes it much easier for printing the various files individually or in groups. The library components available in the project library may also be printed. Each file to be printed may be previewed and the printing scale may be changed as required.

SPICE Netlist Import

This utility allows to import both circuit (.cir) and subcircuit (.sbc) files to the system. The Schematic diagram is generated by converting the imported file data to the project. All the Instance parameters and Model parameters are set during conversion. The circuit is also set for various analyses. All the parameters are set for various types of analysis, which is specified in the circuit file. This routine deletes the currently loaded project upon start. Hence it is to be ensured that the database is saved before invoking this application.

This module may be invoked from Project Explorer in the following ways.

- Right click Project and select ***Spice Netlist Import*** from the list.
- Select ***Spice Netlist Import*** from the task list or from the task toolbar.

 *By default, system does not display the task toolbar. It may be enabled from View menu in the Project Explorer.*

The system asks for saving the project. Then a window opens to select the mode for importing the files. The imported files may be created as a new project or as new hierarchies in an existing project. Select the mode. The Spice Netlist Import window

opens up. Spice Netlist Import collects all the parts information in the library at the time of form load. It keeps a table of this information for extraction of parts while importing. Select File | Open. A dialog box pops up from where the required .cir or .sbc file can be selected. The project is named after the file imported. The circuit file may be viewed in a file viewer. Click the VIEW FILE button.

While importing, there are two modes for part selection.

Automatic: In this mode the system searches and selects the component from library search sequence that matches the criteria in the circuit file definition and loads it to the project.

Manual: In this mode system lists all the parts satisfying the conditions are listed in a table, from which user can select one. The user may choose any component from the list. Similarly for all the definition of various components in the circuit file, several components are listed. The selected components are loaded to the project.

If none of the parts in the library satisfies the search criteria, then system asks the user whether to create a dummy part to keep the Netlist correctly. Or user can ignore this part creation and the related nets remains partially connected. Dummy parts created can be recognized by their formatted names.

In case of subcircuits also system creates a part and assigns the corresponding hierarchy to this part automatically. Parts like this also appear with formatted names.

All information like node modifiers, instance/model parameters, transient initial conditions, Initial node voltage guesses, set up for all types of analysis etc are read from the file and put into newly created project. All instance/model parameters having a spice name are successfully imported.

 *SAVE, .PRINT, .PLOT commands are ignored.*

Netlist/ Wirelist Export & Import

This utility holds all Export/ Import/Conversion operations that can be performed in EDWinXP to switch between EDWinXP and some foreign formats.

This module may be invoked from Project Explorer in the following ways.

- Right click ***Project*** and select ***Netlist/ wirelist Export & Import*** from the list.
- Select ***Netlist/ wirelist Export & Import*** from the task list or from the task toolbar.

 *By default, system does not display the task toolbar. It may be enabled from View menu in Project Explorer.*

Netlist/ wirelist Export and Import window appears as shown in Fig 2.50.

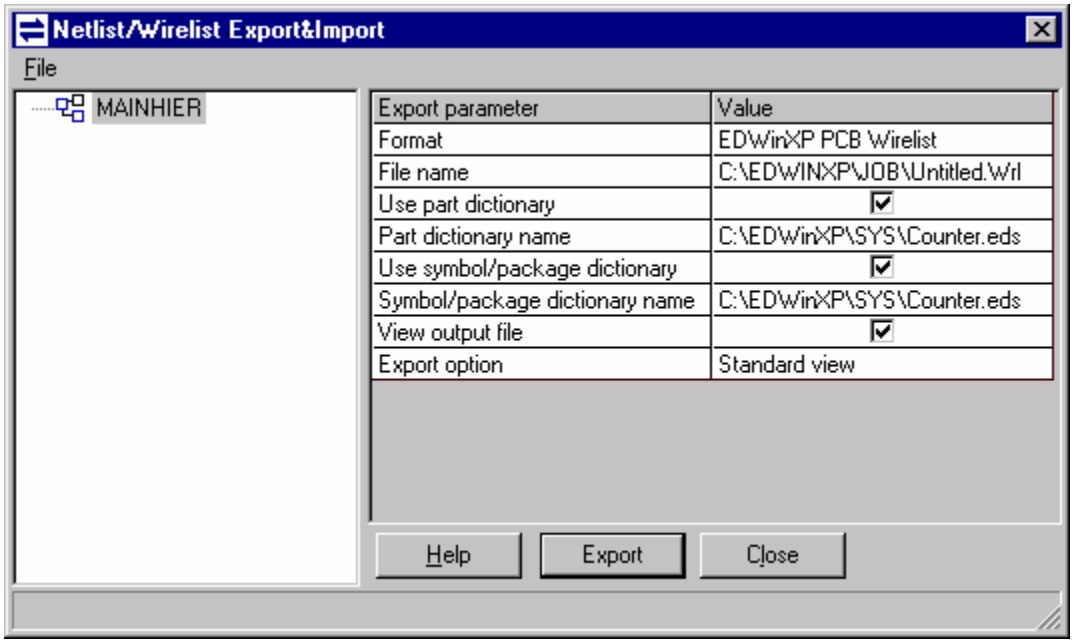


Fig: 2.50 Netlist/ Wirelist Export and Import

Select the required format from the drop down list to which the current loaded Project is to be exported. To cross-match between EDWinXP and foreign formats, a file is required where the alias name is referenced. This file is the dictionary file, which user has to create. For more information on Dictionary files refer the online help of EDWinXP.

File

Export Projects

1. EDWinXP PCB Wirelist

Select Export menu from File and browse EDWinXP PCB Wirelist from the list of export. Browse the dictionary file for the package/ parts and point to the location where the output file should be. To export the contents, click the Export button. A dialog opens were the output file (*.wrl) is saved.

2. EDWinXP Schematic Netlist

This is a new Export facility where the Schematic netlist of the selected project is exported. The dictionary file and the location of the output file is browsed using the ellipsis. To export the contents, click the Export button. A dialog opens were the output file (*.wrs) is saved.

3. EDIF V2.0 Schematic

Select this format and choose either of the following options.

Schematic Netlist only – use this if only the netlist needs to be exported.

Schematic diagram and netlist – use this if the schematic and the netlist have to be exported.

The dictionary file (*.eds, *.edd) and the location of the output file is browsed using the ellipsis. To export the contents, click the Export button. A dialog opens were the output file (*.edf) is saved.

4. Orcad PCB II Wirelist

This option exports the wirelist of the current project to the format accepted by OrCad. Select this option from the list of Export and point to the location where the output file should be. To export the contents, click the Export button. A dialog opens were the output file (*.net) is saved.

5. Scicards Schematic Netlist

This option exports the netlist of the current project to the format accepted by Scicards. Select this option from the list of Export and point to the location where the output file should be. To export the contents, click the Export button. A dialog opens were the output file (*.net) is saved.

 *For all types of export, the output format file is displayed in an ASCII viewer if View Output File is checked. The contents of the hierarchy may be exported by just clicking on the hierarchy and selecting the required output*.

6. CUPL Netlist

This option exports the netlist of the current project to the CUPL format. Select this option from the list of Export and point to the location where the output file (*.pld) should lie. To export the contents, click on the Export button. If the check box for View output file is active, the file is displayed in EDWinXP Viewer.

7. Xilinx Netlist

This option exports the netlist of the current project to the XILINX format. Select this option from the list of Export and point to the location where the output file (*.edn) should lie. To export the contents, click on the EXPORT button. The file is displayed in EDWinXP Viewer if the check box for View output file is checked

Activate Insert I/O buffers if the selected vhdl module is the topmost module of the design.

EDWinXP can output to the following Xilinx output formats

1. Xilinx 3000 series
2. Xilinx 4000E series
3. Xilinx 4000X series
4. Xilinx 5200 series
5. Xilinx 9000 series
6. Xilinx Spartan series
7. Xilinx SpartanXL series
8. Xilinx Spartan2 series
9. Xilinx Virtex series
10. Xilinx VirtexE series
11. Xilinx Virtex2 series

 *The target FPGA place-and-route software is Alliance 2.1*

8. JEDEC Netlist

Export the netlist of the current project to JEDEC format. Select this option from the list of Export and point to the location where the output file (*.jed) should lie. To export the contents, click on the Export button. The file is displayed in EDWinXP Viewer if the check box for View output file is checked Activate Map output file name to view the assignment of VHDL ports to the physical pins of the target PAL device.

EDWinXP can output to the following JEDEC output formats

1. 16L8
2. 16N8
3. 16R4
4. 16R6
5. 16R8

9. ALTERA EDF

Export the netlist of the current project to ALTERA EDF format.

10. EDWinXP RINF Netlist

Export the netlist of the current project to EDWinXP RINF Netlist format. Select this option from the list of Export and point to the location where the output file (*.net) should lie. To export the contents, click on the Export button. If the check box for View output file is active the file is displayed in EDWin Viewer.

Import Projects

1. EDWinXP PCB Wirelist

Select Import menu from File .This option is used to import the wirelist files (*.wrl) and can be used to construct the project database. The dictionary file and the location where the import file resides are browsed using the ellipsis. To import the

contents, click the import button. This action clears the current loaded database. The report file is displayed in an ASCII viewer.

2. EDWinXP Schematic Netlist

Here the Schematic netlist (*.wrs) is imported. The dictionary file and the location where the import file resides are browsed using the ellipsis. To import the contents, click the import button. This action clears the current loaded database. The report file is displayed in an ASCII viewer.

3. Orcad PCB II Wirelist

Select this option from the list of imports which is used to import the wirelist file (*.net). Browse the dictionary file using the ellipsis and point to the location where the import files resides. To import the contents, click the import button. This action clears the current loaded database. The report file is displayed in an ASCII viewer.

 *For all types of import, the input format file is displayed in an ASCII viewer if View Input File is checked. The contents may be imported directly to the hierarchy by clicking on the hierarchy and selecting the required import.*

4. VHDL compile and Import

Select this option from the list of imports which is used to import the VHDL file (*.VHD). Browse the dictionary file using the ellipsis and point to the location where the import files resides. To import the contents, click the import button. The report file is displayed in an ASCII viewer.

Only VHDL that conforms to Level-0 synthesis syntax and semantics can be imported to EDWin. For more information regarding the syntax definition, please go through the file in: \ EDWinXP\ Lib\ Level_0.pdf.

5. ALTERA EDF

Select this option to import a netlist of ALTERA EDF format.

Converters

1. EDWinXP Schematic netlist to CUPL netlist

Converts an EDWinXP Schematic netlist created by VHDL compiler to CUPL netlist.

2. EDWinXP Schematic netlist to XILINX netlist

Converts an EDWinXP Schematic netlist created by VHDL compiler to XILINX netlist.

3. CUPL netlist to JEDEC netlist

Converts CUPL netlist to JEDEC netlist.

4. EDWinXP Schematic Netlist to ALTERA EDF

Converts EDWinXP Schematic Netlist to ALTERA EDF

5. ALTERA EDF to EDWinXP Schematic netlist

Converts ALTERA EDF to EDWinXP Schematic Netlist

Import ODB++ Job

This feature allows importing projects of CAD packages which supports ODB++ formats to EDWinXP.

Import of each ODB++ job step consists of three phases. These phases are as follows.

- The program reads EDA part (packages, components and netlist).
- Geometrical features (positive polarity only) of board layers are imported.
- The reconstruction of read data into editable EDWinXP database objects (This stage is optional).

The geometrical elements (traces, footprints, and copper areas) in phase 2 is stored as packages in project library, separately for each layer. These packages are placed on the board as components. Since packages can be edited in Library Editor, it is possible to modify PCB design in this way and generate manufacturing outputs.

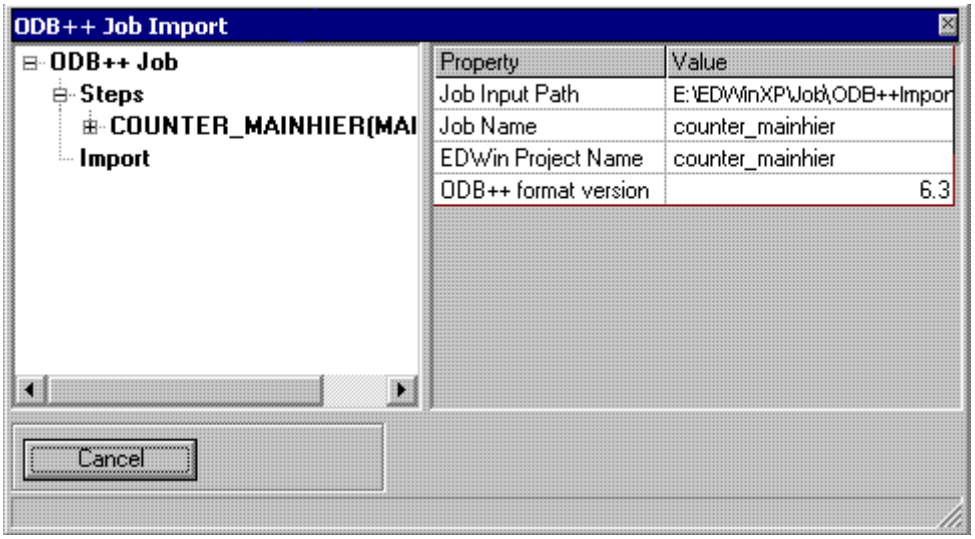
During reconstruction phase, graphic elements stored in packages are converted into traces, via holes pad stacks and pad stacks for component footprints. The program relies on EDA information imported in phase 1 and their links to individual features. Each successfully converted item is removed from the package. Some of the imported features may be left over in packages after reconstruction because there was no clear information linking them to individual objects (like nets, components or packages). These may still be edited, output or used as templates.

Invoking ODB++ Import:
This module may be invoked from the Project Explorer in the following ways.

- Right click Project and Select Import ODB++ Job from the list.
- Select Import ODB++ Job from the task list or from the task tool bar.

ODB++ Job Import window appears as shown below.

Specify the folder containing ODB++ job folder structure in the **Job Input Path** field. By default, the program will import every step specified in the job matrix as a circuit within one EDWinXP project. Importing program accepts ODB++ jobs in decompressed form. User has an option to exclude any step from import. Job names are assumed as project names and step names as circuit names. Since ODB++ does not include any information enabling to reconstruct schematic diagrams, therefore import produces only PCB layout.



Select Import on the left pane. Click on the **Import** tab. Imported output can be obtained from Layout Editor and Fabrication Manager

Project Version Control

Project version control enables storing of different versions of a project in the same disk file. Current version may be saved at any time and all saved versions become part of the same project database. Any saved version may be restored immediately and set as current.

Since all recorded versions are included in the same database and are loaded from and stored in a single common disk file, there is no need to keep track of different version files and worrying about backups. It would be enough to back up only one file containing all recorded versions. It also allows to reconstruct single project database with several versions that were stored as separate database files (.epb) in previous versions of EDWinXP. There are provisions to view general and statistics information's and also to compare selected version with the active version.

Functions of Project Version Control

Archive: Archives selected version.

Restore: Restores selected version as active.

Delete: Deletes selected version.

Edit Remarks: Allows editing remarks for selected version.

Rename: Renames the selected version.

Load Project: Allows to select and load epb/epx files as project version. This function may be used to reconstruct single project database with several versions that were stored as separate database files (.epb) in previous versions of EDWinXP.

Save project: Allows saving selected version as project .epb

General Info: Gives information about Package, Parts, Nets, Buses, Layout Components and Schematic Components of the selected version.

PCB Statistics: Displays information related to the board such as board dimension, number of components, pads, holes for pins, via holes, total holes etc of the selected project version. This also gives information about the layer usage such as layer name, number of trace segments, pad items and copper items in each layer

Compare: Displays the difference between the selected and active project versions.

Circuit

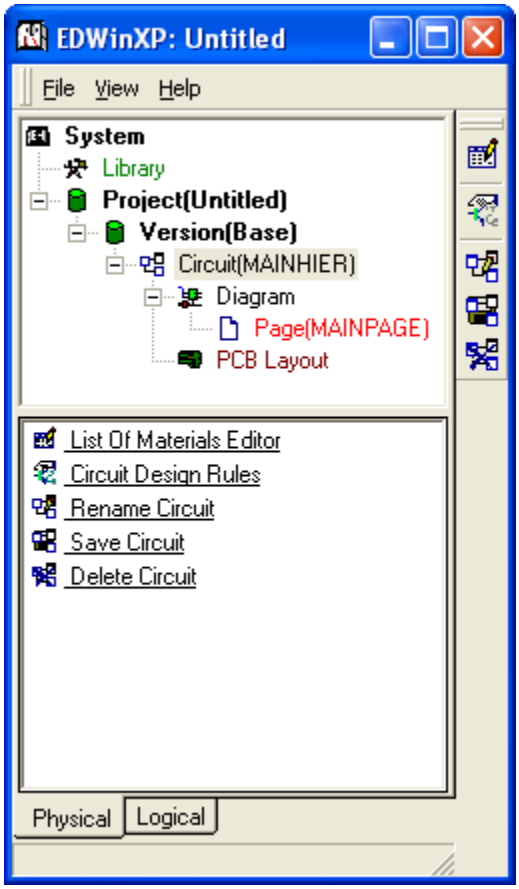


Fig: 2.51

List of Materials Editor

List of Materials Editor creates List Of Materials (Bill Of Materials) of all components in the current project. Apart from components name, various other information's such as Parts name, component values etc of the components may be added to the list. The user has a possibility to select what kind of information about the components he needs in his list as well as the sequence in which these information should appear in the lines of the list.

List Of Materials may be sorted according to the selected field (component names, part names, values etc.). The generated list may be previewed and subsequently, output to the ASCII file. The purpose of the ASCII file is to enable import of list of materials to other software packages - for example EXCEL - to form worksheets for final edition end printing.

You can add additional information's about the component like prices, component manufacturer names etc in List of materials. For this the List of Materials Editor combines the information about the components, which are accessible from the project with information retrieved from user-defined External Info Database (EID)

Circuit Design Rules

You can set certain default Design Rules to work with EDWinXP. This utility is used to preset certain parameters for manual, semiautomatic and automatic routing of traces and component placement. With the given parameters, the Layout conducts a design rule check and any problems are marked by an Error label. The errors may be queried using the Redraw/ Error. The design rule settings may be saved as a permanent setting or may be set for the circuit or for the current project only. The design rule settings may be saved as a permanent setting or may be set for the circuit or for the current project only.

Rename Circuit

To rename the selected circuit of the current project.

Save Circuit

To save the selected circuit of the current project.

Delete Circuit

To delete the selected circuit of the current project.

Diagram

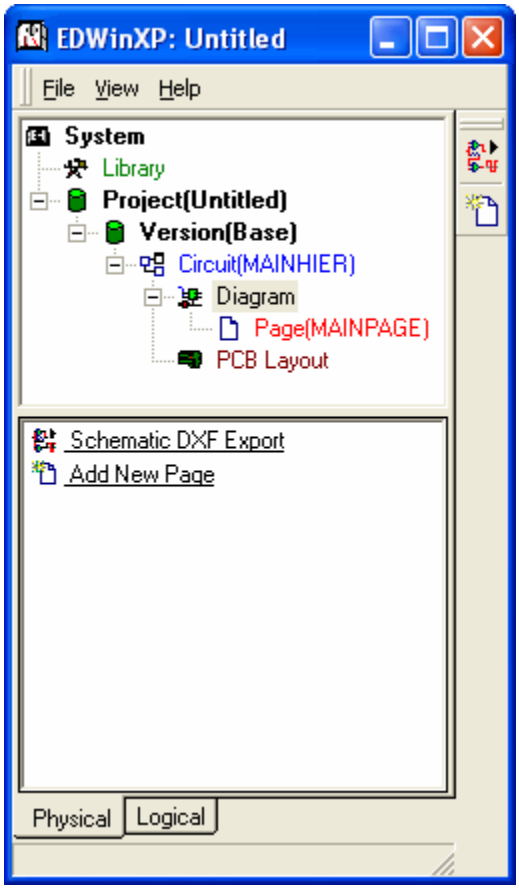


Fig: 2.52

Schematic DXF Export

The Schematic DXF Export is an application that allows to export the Schematic graphics to DXF format.

This module may be invoked from Project Explorer in the following ways.

- Right click Diagram and select ***Schematic DXF Export*** from the list.

The Schematic DXF Export window appears as shown in Fig.2.53

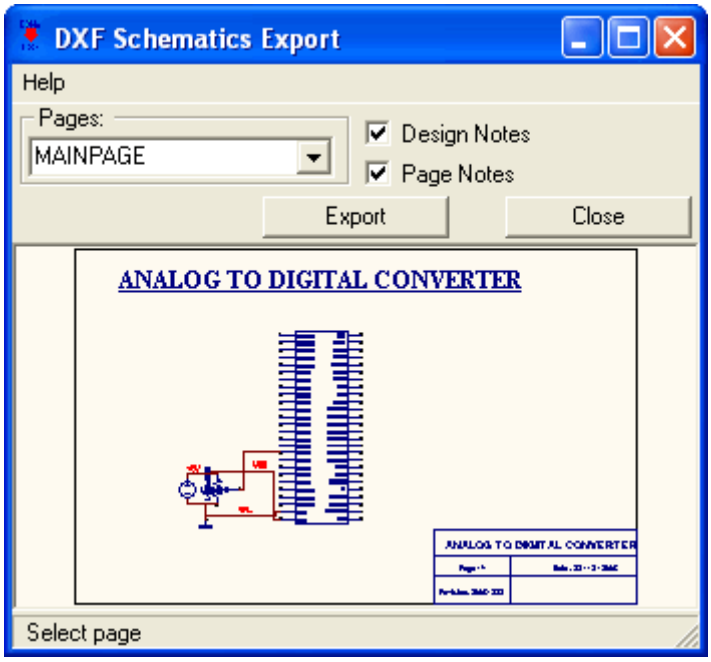


Fig.2.53

A brief description of different options in the window are given below

Export

This exports the Schematic graphics to .DXF format. The exported schematic is saved as a .DXF file.

To export graphics in selected page and to include Design notes and Page notes, check the respective check boxes. On clicking EXPORT a Select Output File: dialog box pops up where the name of the .DXF file is to be entered. Click OK to execute the export. The message displayed in the status bar, while exporting, indicates which part of the operation is being carried out. Finally the status bar displays the message 'DXF Export File Saved O.K., ' which indicates that the export is completed.

Page

Allows to select pages for exporting.

Design Notes

Allows including design notes while exporting.

Page Notes

Allows including page notes while exporting.

Add new page

Creates new pages in addition to the MAINPAGE. Additional pages are usually created when the space to draw a circuit diagram is insufficient on a single page, or when a diagram is required to be drawn as blocks such as input unit, output unit. This splitting of diagram is helpful in validating the circuit.

Up to 99 sheets of maximum size of 4x4 m2 may be created. The name of the page is restricted to 15 characters and a name with spaces is not allowed.

Page [Main Page]

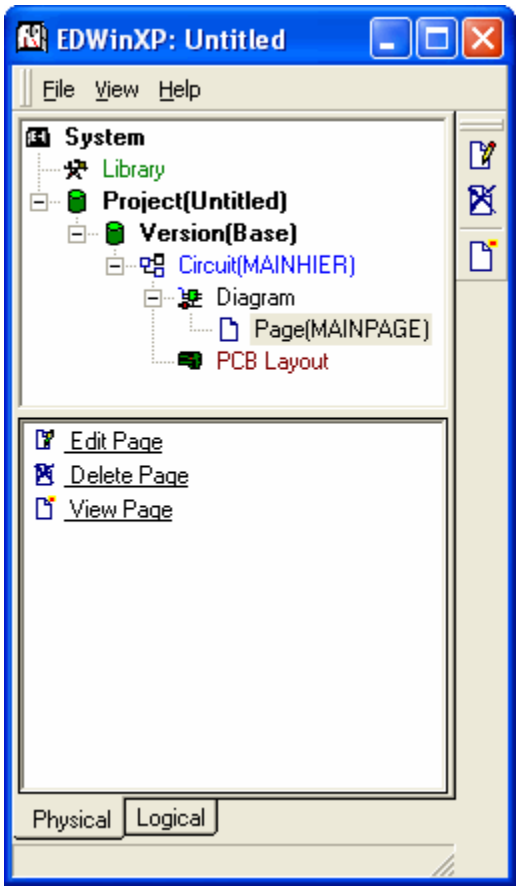


Fig: 2.54

Edit Page

An individual project supports circuits with multiple hierarchical levels with multiple pages within a hierarchy. Part symbols are placed on the pages by "dragging and dropping" from library contents browsers and explorers or by entering part names. Connections are defined either by physically drawing wires and buses or by creating named nets and adding nodes. The netlist is automatically updated when wires and buses are edited. Once the netlist has been created, all wires may be automatically routed from the scratch. Connecting wires are rerouted whenever part symbols are

relocated. Auto placer helps to arrange interconnected part on the page. Packaging routines generate pin-out texts, create part packages and update the netlist. Subsequent design changes are in real time front annotated on the PCB layout. Auto placer includes function to arrange component labels and pin-out text according to user specified design rules.

Delete page

Confirms to delete the selected page other than the MAINPAGE.

View Page

The Viewer shows the schematic diagram of the currently loaded project. This window opens up as shown below.

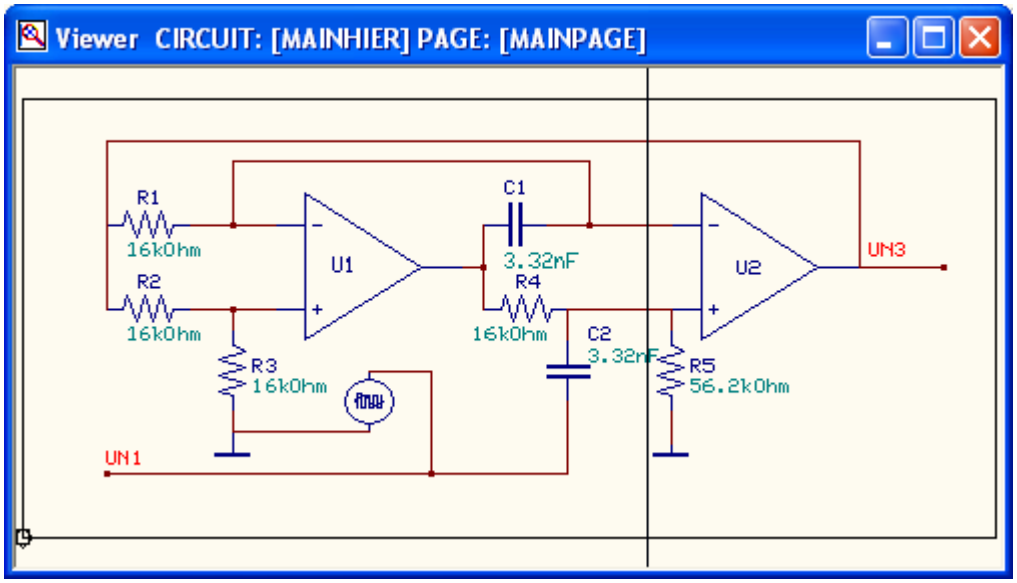


Fig: 2.55

PCB Layout

Edit PCB layout

Layout Editor is used to design the PCB layout of a circuit. The project database supports design of 32-layers boards (28 trace layers, 2 silk-screen & 2 solder masks). The design can be captured either in schematic capture or directly in layout editor. Refer Layout Editor - Page: 210, for more details.

Fabrication Manager

Fabrication Manager provides the options to generate Gerber, NC Drill, PCB Assembly Outputs and Bare Board Test Data required for photo plotting.

Board Analyzers:

Analysis is an important part of any design process. The soundness of a design should be tested to ensure proper functioning of the final PCB. EDWinXP provides two types of board level Analyzers:

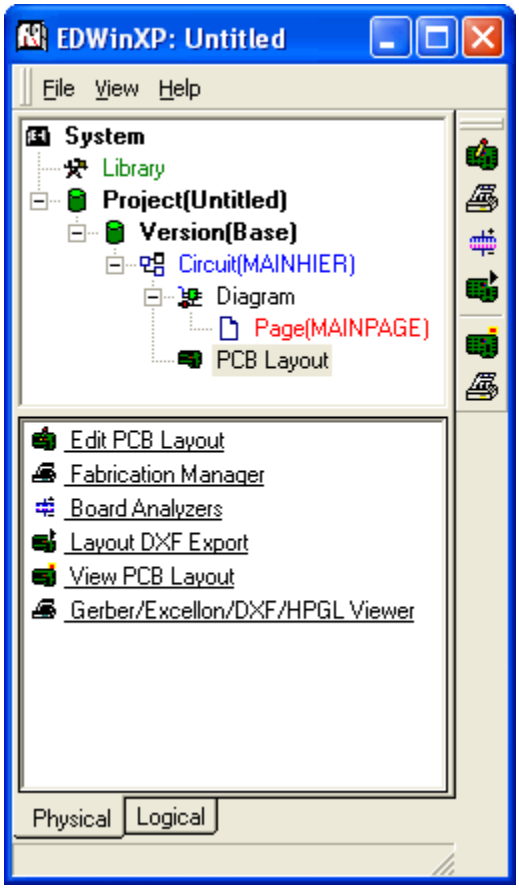


Fig: 2.56

Thermal analyzer

The Thermal Analyzer helps in identifying potential heat distribution problems on the PCB in design stage itself. Refer Thermal analyzer - Page: 237, for more details.

Electromagnetic analyzer

The Electromagnetic Analyzer evaluates the distribution of Electric Field Intensity on a finished PCB. Refer Electromagnetic analyzer- Page: 239, for more details.

Layout DXF Export

The Layout DXF Export is an application that allows to export the layout graphics to AutoCAD DXF format. The DXF file is basically an ASCII file containing necessary vectorial information of the entities present in the layout.

The necessary graphics like copper, texts, traces, 3D-information etc must be selected exclusively from the Parameters tab to export to AutoCAD DXF format.

This module may be invoked from Project Explorer in the following ways.

- Right click PCB Layout and select Layout DXF Export from the list.

By default, system does not display the task toolbar. It may be enabled from View menu in the Project Explorer.

The Layout DXF Export window appears as shown in Fig.2.57.

Parameters tab

The ***Parameters*** tab allows selecting elements of the layout database that are to be exported. The contents of this tab are mentioned below:

General

It consists of a few checkboxes as shown in Fig.2.58, which helps to select certain entities with which the graphic export has to take place. These include:

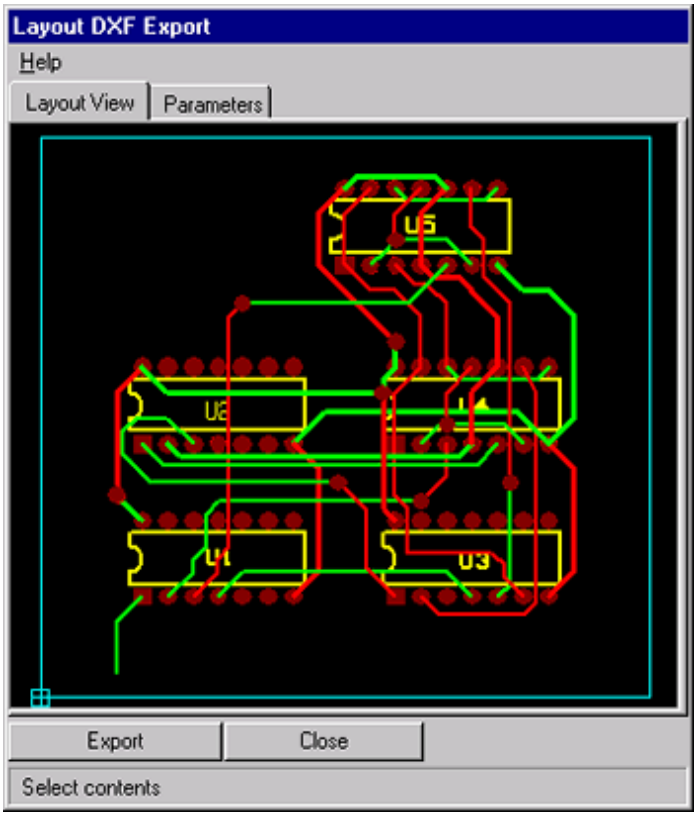


Fig: 2.57

True Size Check this to export graphics in True Size.

Dimensions Check this to include Dimensions while exporting.

Board Description Check this to include Board Description while exporting.

3D Out Check this to include 3D information while exporting. 3D Contents gets displayed only if this option is checked.

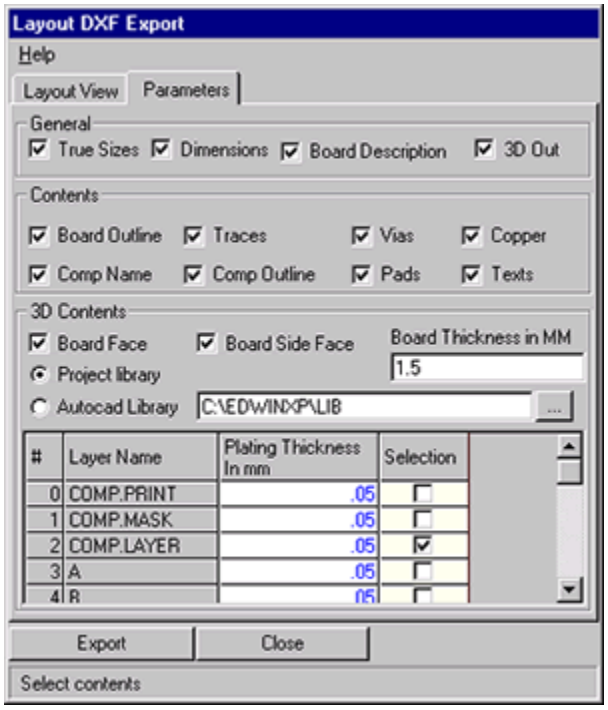


Fig: 2.58

Contents

The various entities that may be exported include Board Outline, Traces, Vias, Copper, Component Name, Component Outlines, Pads and Texts. To export any of these entities, just enable (check) the respective checkbox.

3D Contents

All the 3D information that has to be exported may be set using the controls grouped under 3D contents. These include:

Board Face Check this to include board surface while exporting.

Board Side Face Check this to include board side surfaces while exporting.

Board Thickness in mm Enter board thickness in the textbox provided. The maximum board thickness allowed is 25.4mm. The value entered here gets reflected in the Layout Editor as well.

Project Library Enable this to allow the layout entities to pick necessary 3D information from Project library while exporting. The 3D information gets appended to the DXF file.

AutoCAD Library	Enable this to allow the DXF file hold links to external files having 3D information of the packages (*.dwg, AutoCAD drawing file). The path of these external files is picked up from the default library path set in options. However, user can also select the path of external files from the file selector dialog.
Layers	Layers to be exported may be selected by checking the respective checkbox. Also the thickness of copper items may be selected from the drop down list under Plate thickness in mm for each layer.

 *By default the component print & solder print layers remain selected and they cannot be unchecked.*

Export

This exports the selected graphics from layout to AutoCAD DXF format. The exported layout is saved as a .DXF file.

Operation

Select the entities to be exported from Parameters tab and click EXPORT button. On clicking EXPORT a Select Output File: dialog box pops up where the name of the .DXF file is to be entered. Click OK to execute the export. The message displayed in the status bar, while exporting, indicates which part of the operation is being carried out. Finally the status bar displays the message ' DXF Export File Saved O.K.' which indicates that the export has been completed.

View PCB Layout

The Viewer shows the layout diagram of the currently loaded project.

Gerber/ Excellon/ DXF/HPGL Viewer

Opens ***Fabrication Graphics (Gerber/ Excellon/ DXF/ HPGL)*** Viewer & Import window that permits the user to import and view the Gerber ASCII files, DXF, HPGL, and Excellon files for viewing and validating purposes before photoplotting.

Special function incorporated in the viewer converts imported data to import categories that may be edited in Fabrication Manager prior to reconstruction of projects from graphics. The viewer has the capability for automatic distribution of imported data to most suitable category.

Chapter 3

Library Editor

Library Structure

The library system may be divided into two main parts

1. Part Library
This is the main source of information of components and is accessed whenever new components are added to the captured circuit.

2. Simulation Library
Each simulator and analyzer has its special library or libraries. Various elements in these libraries are accessed upon request depending on currently executed type of simulation/ analysis. The library elements in these two main parts are linked together. Typical example is *Simulation Function*, which is encoded in symbol (part library). ***Simulation Function*** instructs simulator, which model (model library), should be used, to simulate circuit element the symbol represents.
Interconnections between different parts of library system are explained in Fig. 3.1.

Library Organisation

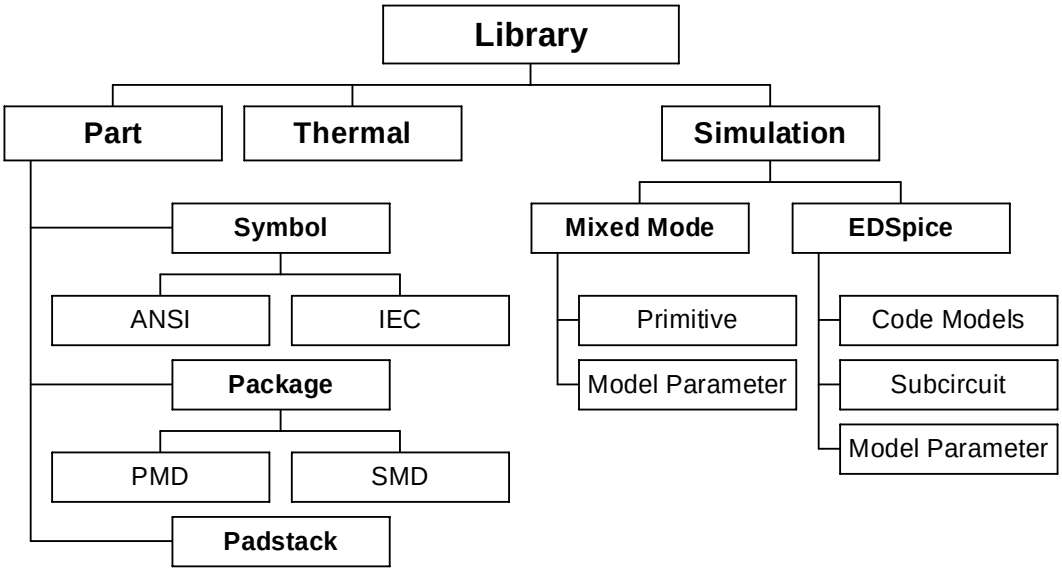


Fig.3.1 Library Organization

Part Library consists of following sections:
Part library files (*.PART) containing parts - *part descriptions*. Each part is associated with a symbol(s) and one package or with either symbol/ package.

Symbol library files (*.SYMBOL)
Package library files (*.PACKAGE)
Padstack library files (* .PADSTACK)

Simulation Library consists of following sections:

Mixed Mode Simulation Models (* .DLL)
EDSpice Code Models (* .DLL)
EDSpice Subcircuits (* .SBC)
EDSpice Model Parameters library files (* .Sparam)
Mixed Mode Model Parameters library files (*.Mparam)

Part Library

Library files are divided into four categories of disk files - the Part library files, the Symbol library files, the Package library files and Padstack library files.

- The **PADSTACK LIBRARY** contains different types of ready-made padstacks that may be used while creating new packages.
- The @TOOLS.PACKAGE library file contains symbols for representing different hole diameters on NC-drill Template drawings. The user may edit these symbols if other shapes are required.

Fig.3.2 illustrates how Part library structure is used in - The Component Create Process.

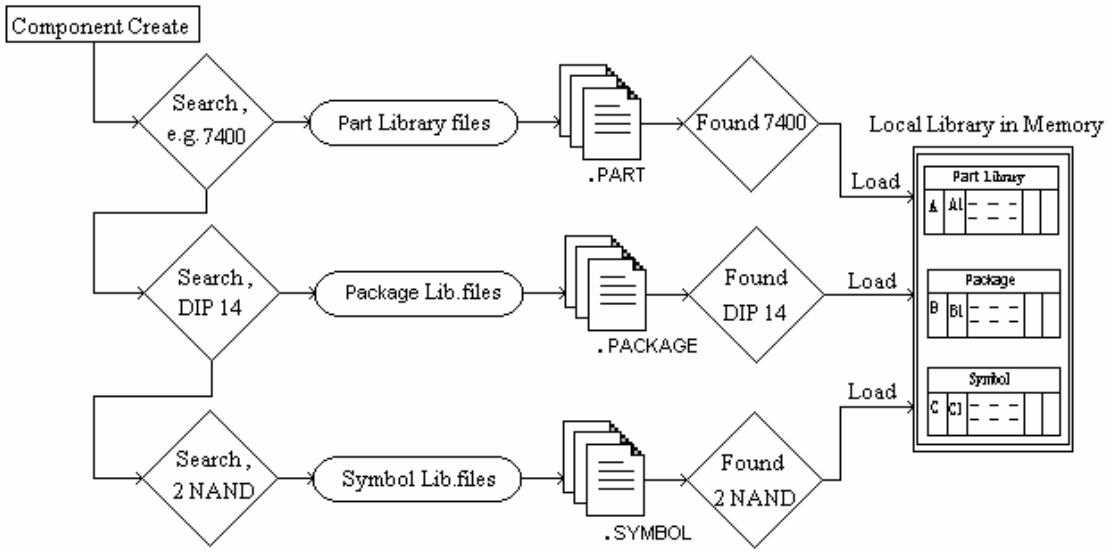


Fig.3.2 Component Creation Process

The libraries *.PART, *.SYMBOL and *.PACKAGE contain the respective parts, symbols and packages. Though the user cannot alter the system library, they can create their own new libraries.

ANSI or IEC Symbols

During installation of the EDWinXP, the user has an option to select one of two sets of symbols library - ANSI or IEC Standards.

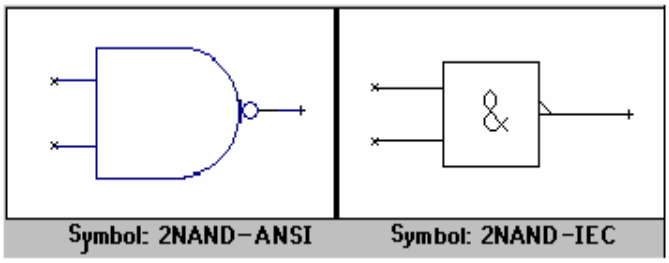


Fig.3.3 ANSI or IEC Symbols

Symbol representation of 2 input NAND gate – ANSI and IEC 2standards is shown in Fig.3.3.

- The symbols library files (*.SYMBOL) with names starting with "A_" contain symbols created according to ANSI standard (for ex. A_TI.SYMBOL).
- The symbols library files (*.SYMBOL) with names starting with "I_" contain corresponding symbols created according to IEC standard (for ex. I_TI.SYMBOL).

Structure of Part, Symbol, Package and Padstack

Symbols and packages are created independently and saved as *.symbol and *.package. These symbol/packages can then be assigned to a *.part file.

Part Structure

The Part library contains Package and corresponding Symbol attached. In earlier versions of EDWin, (EDWin 16 and EDWin32), Components are loaded on the database as Parts or Symbols or Packages (where components placed only as symbols/ packages are mainly used for simulation/ mounting pins). But now all components created in the Project are referred to as Parts, i.e. symbols/ packages used for simulation purposes/ mounting holes respectively are now created as SPECIAL PARTS where the part may either have symbol or package.

2. IEC - International Electrotechnical Commission 2. ANSI – American National Standard institute

Even though (unlike EDWin 2000), symbols and packages can be created separately and saved into individual files in EDWinXP, library components can be loaded into a Project only as Parts.

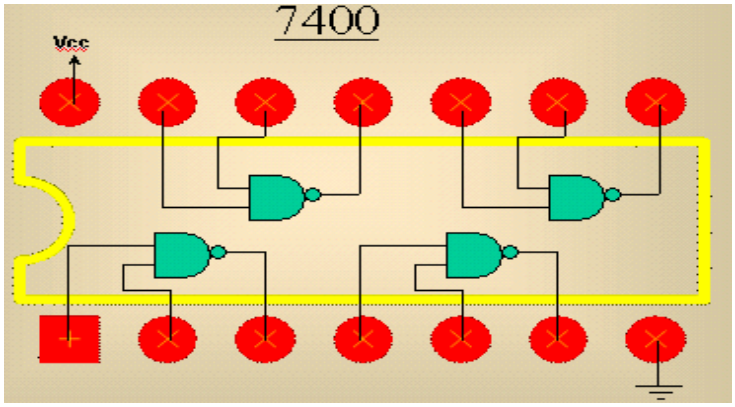


Fig.3.4 Part Structure

The part description contains: **Part name** e.g. 7400 shown in Fig.3.4 contains 4 groups of NAND gates using the package DIP14.

This is not the actual view but this has been constructed to show how a symbol and package are related to form a Part.

Symbol Structure

The symbol is assigned by - Part Editor | Edit | Add Group or simply by drag and drop of a symbol from Library Explorer to the Library Editor. If it is included in the Search Sequence, the corresponding diagram of the symbol is displayed in the preview.

If there are two or more symbols of the same name, the one which is on top of the Search Sequence gets selected. For e.g.: if a user wishes to use 2NAND of A_CUSTOM.SYMBOL rather than A_DGTAL.SYMBOL, A_CUSTOM.SYMBOL should be placed higher up in the Search Sequence.

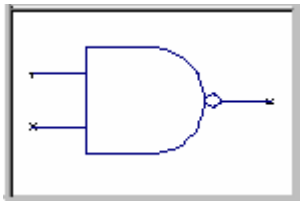


Fig.3.5 Symbol Structure

Symbol name e.g. NAND is shown in Fig.3.5.
If the symbol does not exist or if it has not been included in the Search Sequence, the message "Symbol XXX not found appears. Check whether you have spelt the name correctly. The symbol names are case sensitive".

Package Structure
The package is assigned by drag and drop from Library Explorer to the Library Editor or by just entering the name in library editor. If it is included in the search sequence, the corresponding diagram of the package is displayed in the preview.

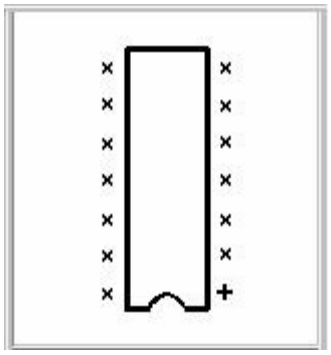


Fig. 3.6 Package Structure

Package name e.g. DIP14/300 is shown in Fig.3.6.

Padstack Structure
Every Component footprint has pins which has physical attributes like diameter (for through hole components) and length/ width (for Surface Mounted Parts). When components are placed on a PCB for connection, these pins must be assigned an area and has to be defined in each of the layers that constitute a PCB. The area occupied by the pins on a PCB is of different shapes and size. Padstack editor serves the purpose of defining the size and shape in each of the layers.

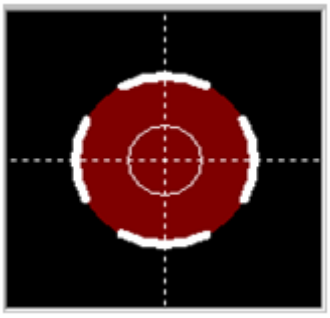


Fig. 3.6 Padstack Structure

Padstack name e.g. P_RND_200_H_88 is shown in Fig.3.7.

Creating Library Elements

In this section, we will see how a 2XOR symbol and DIP14/300 package are created and incorporated to form a 7486 part.

Double click on the task 

Library in the Project Explorer to launch Library Editor.

This module deals with the creation of the following.

Creating Symbols
Creating Packages
Creating Parts
Creating 3D Packages
Creating Padstacks

Creating Parts

From the window that opens up on selecting **Library Editor**, select ***File*** | ***New Part***. Enter the name of the part as 7486 and press Enter.
An example is dealt here, with the assumption that package and symbol already exist. Normally, symbol and package has to be created before starting to fill in information for the part. The details to be specified here are:
Under the General column, enter the following information for the new part.

Name	Name of the part, here it is 7486.
Prefix	Part prefix used for packaging, give it as U.
Description	Enter a brief description about the component, Quad 2 IP XOR.
Manufacturer	Double clicking on this option displays *a Select Manufacture Type* dialog box, which lists different manufacture types. Select the manufacturer name and click **ACCEPT** to include this information.
Technology	Double clicking on this column displays a *Select Technology Type* dialog box from which the standard technologies available may be selected.
Type	Double clicking on this column displays *Select Technology Type* dialog box. The component may be specified to be one among the digital, analog, discrete, or special part.
External Index Code	Add External Index Code to the part which helps to link some external material index in order to fetch additional information about Bill-of-Material, like prices, manufactures name, name of the part in local language etc from the EID (External Info Database).
Part Source Library	Displays the path of the part. For a new part, displays [New Part].

Under the **Package Details column**, enter the following information for the new part.

Package	Package for the part, here DIP14/300, and press Enter
Package Type	Double clicking on this displays a Select Package type dialog box, from which the existing types may be selected.
Package JEDEC Name	Displays the JEDEC name.

Package Source Library Displays the path of the package.

Necessary information regarding the Simulation and Thermal parameters may be entered.
To assign symbol for the part, select **Edit / Add group** and give the Group Name, Symbol and the group before which the symbol has to be inserted (optional) in the pop up text box. Similarly add 4 groups using **Add group** menu item. Groups may also be added by Drag drop from Library Explorer.

So now we have enough information regarding the Part like its package, symbol. The last section to complete the Part creation is to link between the symbols and the package. For this select **Edit/ Edit Pinout** to switch to pin out assigning. The menu items under Edit changes accordingly. Easy way of assigning is using **Edit/ Auto assign**. In the popup text box type 1,1,2,3,1 to complete the assignment for the first two groups similarly type in 3,1,4,3,8 to complete pin assignment for the last two groups.

The **Supply Pins** GND/ VCC is assigned for pin number 7 and pin number 14.

Creating Symbols

The symbol of **2XOR**, shown in the Fig. 3.8, may be created in the following way:

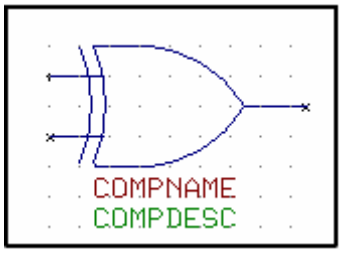


Fig. 3.8 2XOR

1. Double click 

Library in the Project Explorer to launch the **Library Editor**.

2. Select the SYMBOL tab in the bottom. The Editor screen appears with a single entry placed on the screen. This entry is located at X, Y location 0, 0 and its entry number is 1 indicated by the "+" sign. An entry is a point at which the connections to a component pin are made. All other entries added later will have an "x" sign. Along with the first entry, the system also places the **COMPNAME** and **COMPDESC** text. The **COMPNAME** refers to the packaged component's prefix, like U1. The **COMPDESC** is information about the component like 7486, 74LS86 etc. Zoom down for proper visibility. Turn ON the ***Grid*** by enabling the grid from the dropdown  . The value for the grid may be selected from the drop down list as .0500".

3. To create the outline for the 2XOR symbol, click Create Graphic Item tool and select the tool Create line.

4. Click the cursor anywhere on the workspace. A highlighted line appears attached to the cursor. This position will denote the starting point of the line. Click the left mouse button to anchor the line. Move the cursor horizontally along the work space unto a point where the required length for the line is obtained. Press the left mouse button to fix the line at the desired position.

5. Place another line, few grids (8) lower but parallel to the first line.
6. Now draw an arc such that it passes through the ends of the two lines. Select the tool **Set Contact Point**. Choose **Place Point P1** and click on the point just above the end of the upper horizontal line to mark the starting point of the arc and press the left button to place a point there. Similarly place the second point using the tool **Place Point P2** to mark the end point of the arc.

7. Select **Create Arc** from the functional tool **Create graphic item**. Click anywhere near the contact point to get a phantom arc tagged to the cursor. After adjusting the size of the arc, click to place it.
8. Adjust the arc, if necessary, by selecting the **Stretch Item** function tool and click the **Stretch arc radius** tool or press F1 key, to change the radius of the arc. Move the cursor to the inner side of the arc and click. We see the arc's radius expands and contracts with the movement of the cursor.

   Tip: Pressing the SHIFT key while relocating/ stretching an item allows the item to move/ stretch smoothly.
9. Ensure that the arc is of required shape and size. Repeat the same arc using the tool **Repeat Graphic** Item and place it as shown in Fig. 3-9.

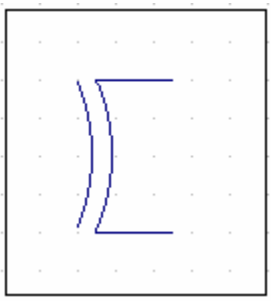


Fig. 3.9 Placing arc using Repeat Graphic Item

10. In the same way draw an arc to define the curved side (near the output pin) of the XOR gate.
11. Place the other arc in the opposite direction.
12. Now select the **Create graphic item** tool and select the option tool **Create line** and join the entry pin to the periphery of the symbol outline using

this line. Since the part of the outline is curved most parts of it do not lie on the grid and hence it will not be easy to stretch the line with the snap settings. The first option is to switch off the Snap (or press SHIFT) and then stretch the line till it reaches the symbol outline. Another (better) option is to change the length of the line using its **Property window**. To do so, first create a line spanning across two grids (0.1000"). Click in the workspace, keep the mouse over the point of the symbol outline where the line has to intersect it and note the X coordinates (using long cursor is recommended so that the X coordinate selected is on the same horizontal level as the line) and then press ESC. Now invoke the property window by selecting the last Function tool **Properties** and the first option tool **Item(s) Properties (F1**) and manually enter the coordinates in End X and press enter. Use the **Repeat Graphic Item** tool to repeat the line and place it on all the three pins.

13. Place the first/ default entry (+) exactly at the starting point of the first pin of the XOR gate using the **Relocate item** tool.

14. We will now place the remaining two entry points Select the Create graphic item tool and click the **Create entry** pin option tool or press F6 key, for creating the entry points. Move the cursor along the workspace to the second input point of the symbol and press the left button. The entry point is placed at the required position and displayed as a small **"x"** .To view the entry number, switch ON the options **View | Symbol | Entry number**.

15. Another way of adding an entry is to use the **Repeat Graphic Item** tool. Click on an entry, a copy of the entry is tagged to the cursor; place it at the output pin.

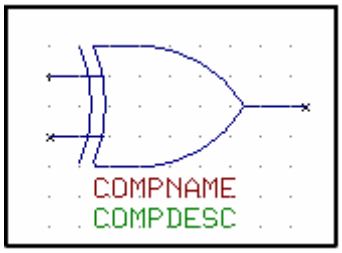


Fig. 3.10

16. Now the graphical construction of the symbol is over and the Simulation Function of this symbol has to be assigned if the primitive DLL is available.

Refer tutorial on Simulation to learn more about Simulation Functions and primitive DLLs.

Select the option tool **Symbol properties** from the function tool **Properties**. Triple click (click thrice in quick succession) on the grid cell adjacent to

Simulation Function, a dialog box as in Fig. 3.11 listing the available Simulation Functions is displayed. Also, it is easier to get the Simulation Function by selecting the checkboxes **Match No. of Pins** and **Digital Models**; a list of all the digital components with the same number of pins appears. Select the one that matches the functionality of the symbol, for the **2XOR** symbol, this is +**528** and press ***ACCEPT***.

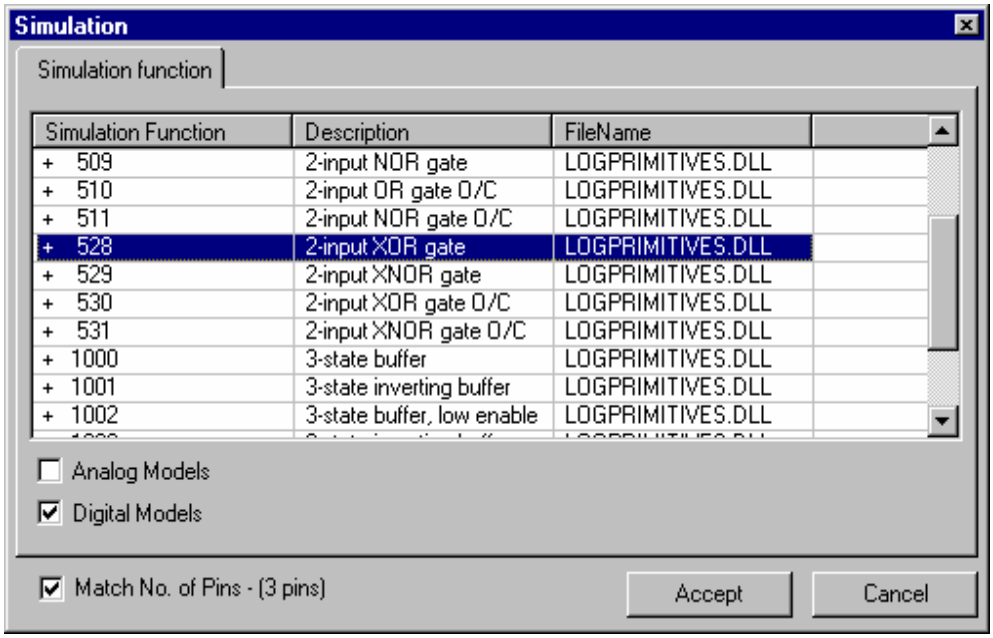


Fig. 3.11 Simulation Function

If the symbol is to be used for SPICE simulation, select the grid cell adjacent to EDSpice Element code and click thrice on it in quick succession (triple click) to launch a dialog as in Fig. 3.12, select the model corresponding to 2XOR i.e. D_XOR and press ***ACCEPT***.

Select **Symbol type** clicking in the grid cell adjacent to it. Browse through the tree view in the sequence Digital | Gate | XOR.

Enter a friendly Symbol description in the grid cell adjacent to it, say 2XOR.

17. Select the  Edit entry attributes tool to give the settings for entries. Click on left top input pin of the symbol created. A dialog box appears containing input text boxes.
    a. **Entry name** - Type IN1 in the text box (any user defined name may be given).
    b. **Sim Name** - Select IN1 from the dropdown list.
    c. **Spice Entry** – Select Input1 from the dropdown list.
    d. **Visible Pinout** – activate check box if the Pinout of the component has to be viewed in the Schematic editor after packaging of the component.
    e. **Swap level** – set to 1.

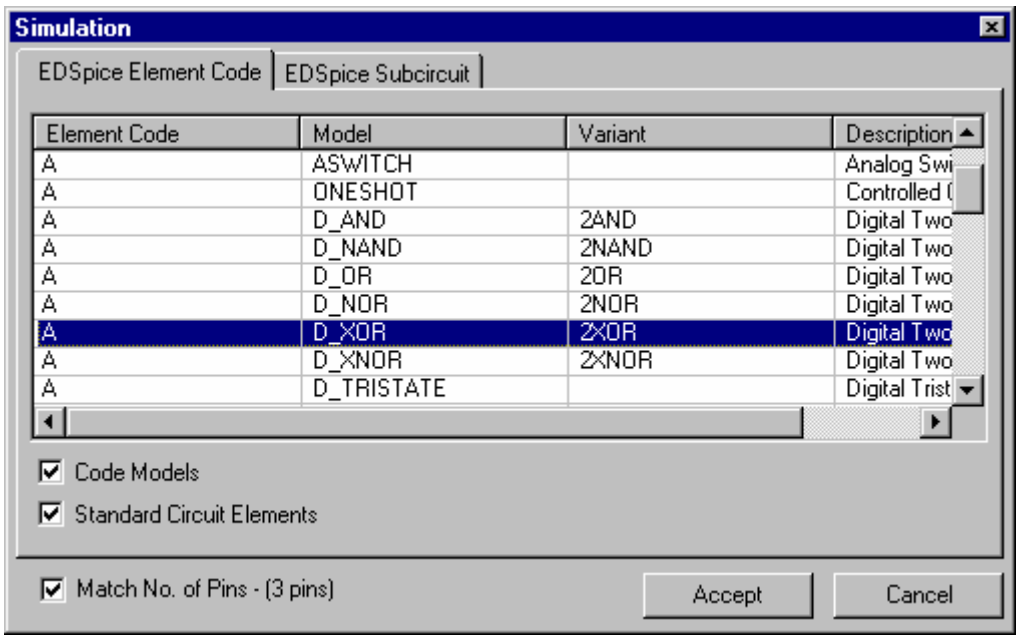


Fig. 3.12

If the Swap level is set to 1, pins may be exchanged with any other pin. If set to –1, swapping of pins is not possible. For e.g., pins 1 and 2 of the XOR gate can be swapped because both are input pins but the output pin should not be allowed to swap. So we set the swap level for input pin of XOR as 1 and that of the output pin as –1.

Click ***ACCEPT*** after completing the settings for the first pin.

Without closing the ***Edit entry Attribute*** window click on the second pin and make settings similar to that of first pin and press ***ACCEPT***. Then click on the output pin, make the necessary settings (set Swap Level to -1) press ***ACCEPT*** and finally press ***CLOSE*** button to return to the workspace.

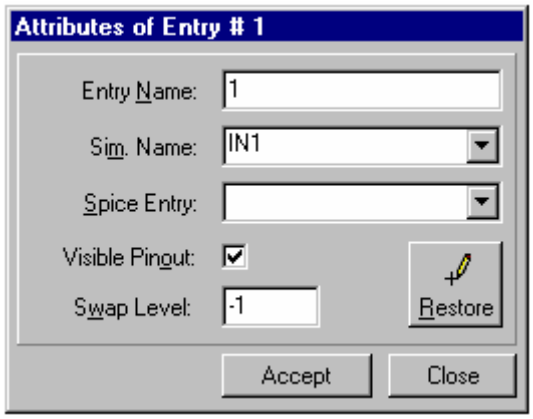


Fig. 3.13

18. After assigning the Simname, we will have to position the COMPNAME and COMPDESC texts. Select the **Relocate** function tool. Click on the text and place it at the required position.

19. The display of PIN ATTRIBUTE (denoted by PA) texts alongside the pins may be enabled using View/ Symbol/ PA Text. Select the  Relocate function tool. Click on the PA Text of the first entry and place it near to the pin. Similarly, the PA Texts for all the other pins may be repositioned.

20. Save the symbol to a disk library. If a new library is created, add it to the search sequence. Return to the Part Editor by selecting the Part tab below.

In the same way symbols for NAND, INV etc. may be created.

Tips: To create an arc without defining the contact points, select  Create Arc from the function tool  Create graphic Item and click on the workspace. A phantom arc is attached to the cursor. Position the other end of the arc (not the cursor end) at the point where the arc should start and click. Stretch the cursor to get the required curve and click to complete the arc.

Library Editor creates the symbols automatically using the Symbol Creation Wizard feature. To auto-create the symbols you have to select the option File / New Symbol using Wizard at the start of creating the symbol.

Creating Packages

The **DIP14/300** (where /300 signifies the pin to pin distance) package, as shown in the Fig.3.14 be created using the following steps.

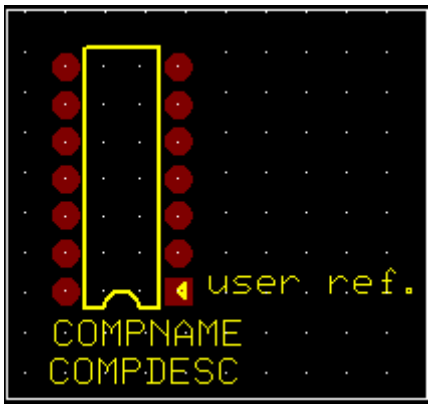


Fig. 3.14

1. Double click 

Library in the Project Explorer to launch the **Library Editor**. To start creating a new package, click the tab PACKAGE to open Package Editor.
2. Select **File / New Package**. A single pin with its dimensions appears on the workspace. This entry is located at X, Y location 0, 0 and its first pin. Each pin of the physical component has a specific size. To assign this size information, we will have to specify a padstack for each pin. Select the Function tool **Change**

Padstack and its option tool **Select Padstack** and click on the workspace to pop up a window as shown in Fig 3.15.

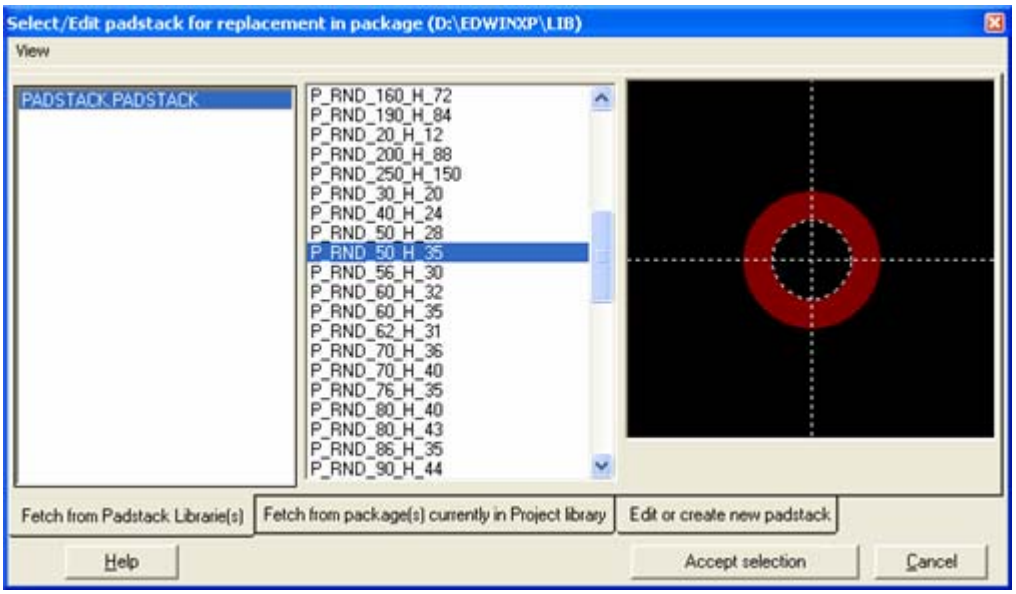


Fig. 3.15

3. Choose an existing padstack **P_RND_50_H_35** and click ***Accept selection***. Now draw a block around the padstack to change to the selected one.

Tip: We may view the actual size of the pin by choosing View | Package | True Size.

4. Select the **Repeat Graphic Item** function tool to repeat the pads. Select **Step Repeat item** option tool to repeat it in steps. Click on the center of PAD/ PIN already positioned. The **Step Repeat** menu will appear and it prompts for the inputs viz. steps, dx, dy. Since DIP14/300 contains 14 pins placed equally on either side, we enter the following information 6, 0, 0.1. Click OK to place pads on one side vertically upwards with the difference of 0.1 inches.
5. Now we will start the second row of pads for the IC. Unselect **Step Repeat Item**, click on the 1st pad and then move the cursor by the inter-pad distance (for DIP14/300 it is 0.3000") and place the 8th pad.

6. Now we may repeat the above step to create another 6 pads of the DIP14. Click on the eighth padstack. The dialog box appears. Type **6, 0, -0.1**. We will find another set of 6 pins have been created.

7. All 14 pins of the IC are placed. We have to create an outline for the part. The outline should be on the Comp. Print layer in board design. Hence this rectangle must be created on this layer. To select the layer on which to create drawing items, go to **Layer | Select Layer | Comp. print** or simply select **COMP.PRINT** from **Layers** toolbar (Toolbar can be displayed by **View | Toolbars | Layers**). This will set the layer as **COMP.PRINT** for creation of graphic elements.

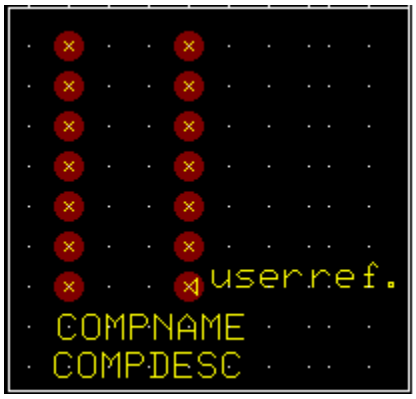


Fig. 3.16

8. Select  **Create Graphic Item** tool and then  **Create line** option tool to create a rectangle border around the pads. Now turn ON the grid, and set the grid and snap size. Click on the workspace. A small line will appear at the cursor. Move the cursor to the point where the graphic should start and press the left mouse button. As we move the cursor, the line is stretched, left click on completing one side. Refer picture below and create the lines 1-2, 2-3, 3-4, 5-6 and 6-1. As per the general convention usually a small curve is present in the outline to identify the starting point of pin numbering. Place contact points on 4 and 5 and create an arc on the outline using the tool  **Create Arc** as shown in Fig.3.17.

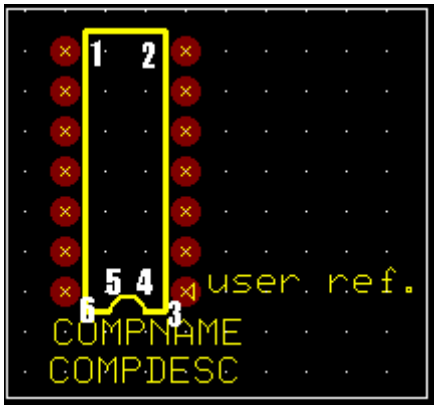


Fig. 3-17

9. The IC's first pin is generally a square pin. This is to help identification for assembly. We will then have to change the shape of pad for pin 1. Change the padstack assigned to this pin from P_RND_50_H_35 to P_SQR_62_H_35. For this, we will first have to select the  **Change Padstack**. Press F1 key and click on the padstack (First one) which is to be changed. The **Select Padstack** window pops up. Select the tab **Padstack**. Choose the required padstack, here it is P_SQR_62_H_35. Click ***SELECT*** to return to the workspace with the padstack replaced. Pin 1 is now a square pin.

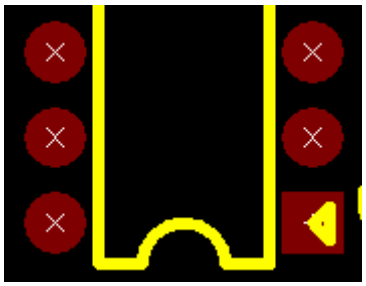


Fig. 3.18

10. Enable the  **Relocate** function tool and click on the COMP NAME text. We see that the text gets tagged to the cursor. Drag and position it near the top of the symbol at the left top corner. This defines the position for the component designator in the layout.
11. Select **File menu | Save Package** and save it to a disk library.

Creating Padstacks

Now we will see how to create a padstack RND_PAD, as shown in the figure below, using the following steps.

Fig. 3.19

1. Double click 

Library in the Project Explorer to launch the ***Library Editor***. Click the tab PADSTACK to open padstack editing mode.

You may create the padstack using two ways. Either by entering the padstack details using the wizard or by manually editing the default padstack in the workspace.

Creating a new padstack automatically

1. Select **File | New Padstack using Wizard**. to pop up window as shown in Fig.3.20.

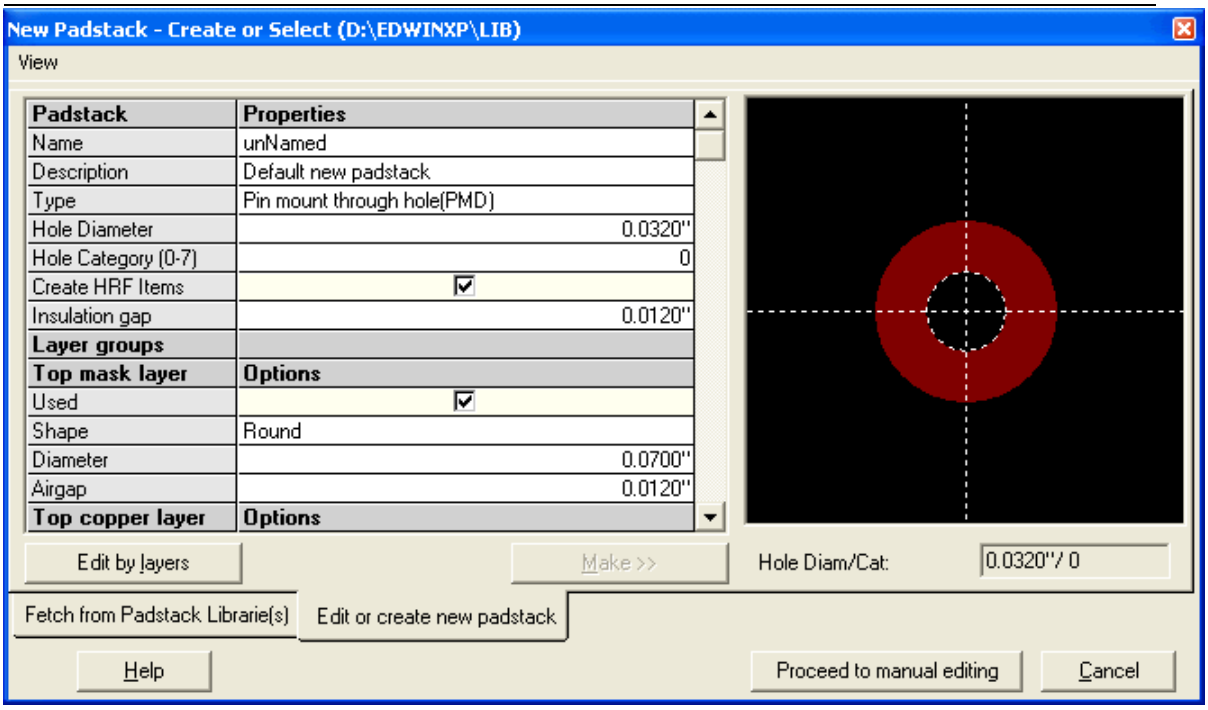


Fig. 3.20

2. In the window, a miniature representation of the padstack is shown in the preview. Right click on the preview for options to view True size, Hrf items and Airgap view. From the **Fetch from Padstack Library(s)** tab, select the padstack "N_RND_100_H_100". Now on moving to the **Edit or Create New Padstack** tab, the padstack details of "N_RND_100_H_100" appears.

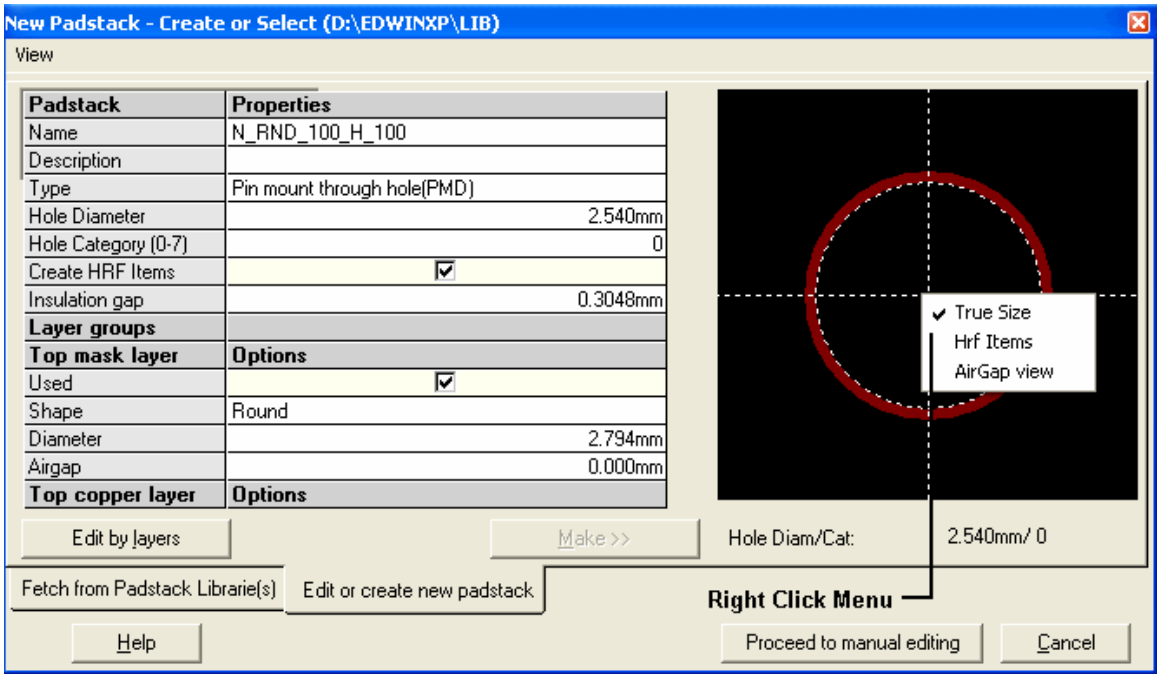


Fig. 3.21

The minimum information required to create a New Padstack is given in the Fig.3.21. The user may edit the values

Name = N_RND_100_H_100 and press the <enter> key.
Create HRF items = select the checkbox
Airgap = 0.0120"
Hole Category = 0
Hole diameter = 0.1000"

On clicking the ***Edit by Layers*** button, the pad details of different layers (Shape, diameter, Airgap and the option of selecting the layers to be used) appears.

Global Editing of layers is also allowed.

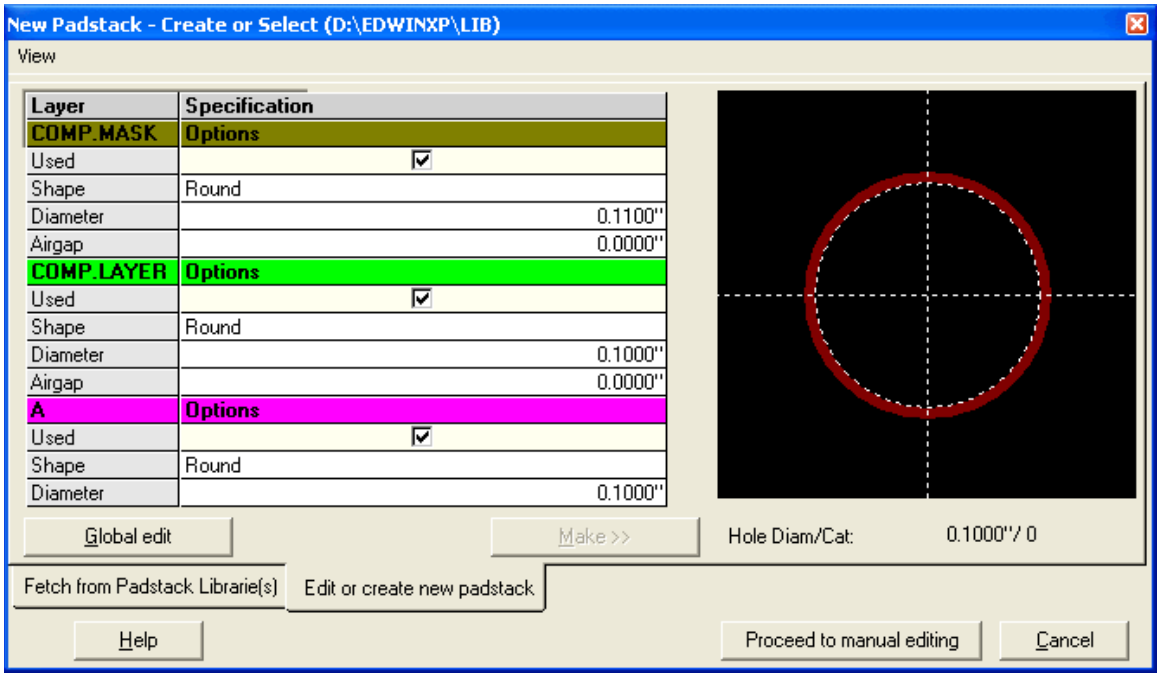


Fig. 3.22

Finally click the button **Make** to create the new padstack. Now the edited changes are visible in the Preview in the right pane. Click on ***Proceed to manual editing*** to effect the changes and exit.
This completes the Padstack creation using wizard. The edited padstack appears in the Padstack editor and further edition can be done using the tools available.
File | Save Padstack | Padstack name.

Create the padstack manually

1. From the **Library Editor /Padstack** tab. (The editor opens with a default new Padstack creating and editing window).
2. Click on ***proceed to manual editing*** button. The editor opens with a new Padstack.
3. Set the hole diameter using the tool **Properties/** **Padstack Properties.** Enter the hole diameter as 0.035" and hole category as 0. On

clicking the ***ACCEPT*** button you may see that the hole is placed on the workspace, indicated by dotted lines.

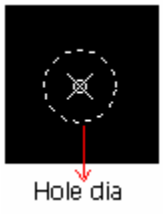


Fig. 3.23

Tip: Zoom up or zoom down to get a clear view of the hole as shown in the figure above.

4. Now you have to create the pad for each layer.
5. Select the **Create Graphic Item** function tool and select the **Create Circle** option tool to create a round padstack.
6. Click the mouse on the workspace. A small circle gets placed on the workspace. To obtain the required size, you have to stretch the circle using the **Stretch Item** function tool.

Tips: Pressing the SHIFT key while stretching an item allows to stretch the item smoothly to any size. Switch off **View/ True size** while selecting an item for stretching or relocating.

Using **Place Contact Points** function tool; you may easily create the circle. Place two contact points P1 and P2 as the start and end points of the diameter of the circle. Then select the **Create Circle** tool and click the mouse. You will see the circle being created automatically enclosing the placed contact points.

Now you have created a single layer pad.

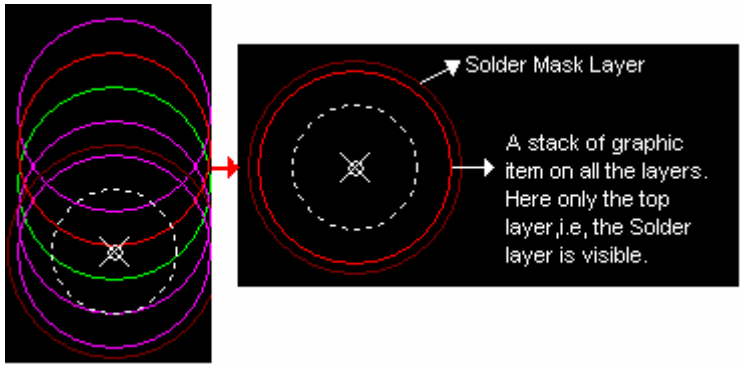


Fig. 3.24

If you want to create the pad for all layers, you have to repeat the graphic item 32 times using the Repeat tool. Press the ESC button or the ESC key to stop the process of repeating items. Then change the layers for each item using the tool Properties/ Item Properties and assign each graphic item to different layers.

Finally keep these items one above the other such that the hole comes in the center of the stack to get a single padstack. Select the Relocate tool to place the circles together.

Usually the diameter of the graphic item for the **Solder** mask layer and **Component** mask layer is kept slightly greater than that for the inner layers. So, in the figure above you can notice that the outer circle (Solder Mask) is bigger than the stacked circles.

Tip: To view any layer in the padstack, select View | Active Layers. A window pops up. Toggle the status of the layer you want to view as YES and keep the status of all other layers as NO. Click *ACCEPT* to return to the workspace with the selected layer displayed.

7. The HRF item may be created using the tool **Create Graphic Item / Create Hrf Pad** along with **Create Arc** tool enabled. Define the contact points with the tool **Set Contact Point**. Then select **Create Graphic Item** with both the tool **Create Hrf Pad** and **Create Arc** tool enabled. Draw arcs to surround the padstack as shown in fig. 3.24.

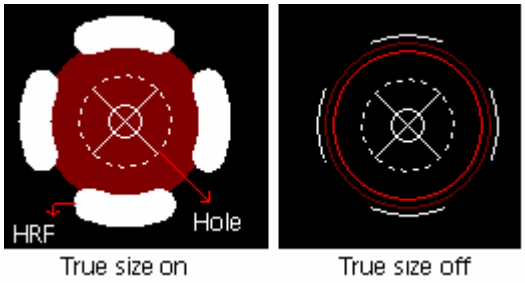


Fig. 3.25

8. Save the padstack by selecting **File | Save Padstack** from the Padstack Editor window. To edit an already existing padstack, select the padstack from Library Explorer and right click to pop up a menu. Select Edit Padstack for editing.

Library Explorer

The function of the tool Library Explorer is to provide the user with the list of available libraries. All library components in each library are displayed irrespective of the libraries added in the search sequence. This is especially useful for copying and moving components from one library to another. Apart from this, user may also place components (included in the search sequence) on the schematic/ layout. You can open the library that contains the file you want to move or copy, and then drag it to the library you want to put it in, provided they belong to the same category.

Similarly, operations performed in the search list of library browser are applicable here. New libraries may be created with much ease.

All the libraries including system and custom libraries will be displayed in the explorer irrespective of whether the custom libraries have been included in the search sequence.

Starting Library Explorer

1. Click on the option tool to open Library Explorer as shown in Fig.3.26.
2. Click on any directory to open up folders. (For e.g.: Part).
3. Click on any of the libraries to display list of library elements present in the selected library.
4. Select the component(s) from the list and drag & drop into the layout editor or Send to/ Layout.

Another copy of the drag and dropped component remains tagged to the cursor unless ESC key is pressed.

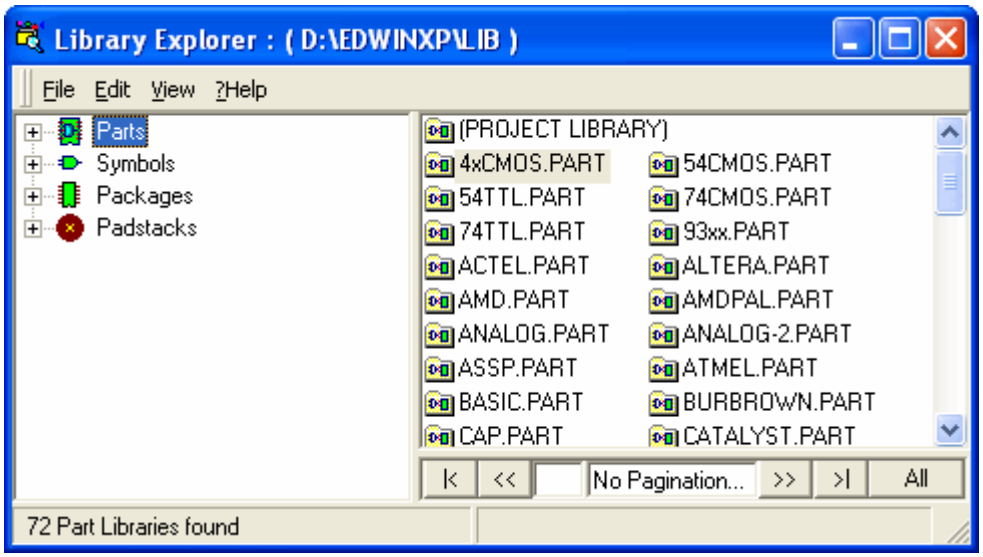


Fig.3.26. Library Explorer

Part Library

Displays a list of part libraries in the Library Explorer window and is mainly used to create new Part libraries, to copy/ move components to different part libraries. Also the symbol and package that comprises the selected part may be viewed using the viewers. Another major use of this explorer is that user may place components on the editors from here.

Symbol Library

Displays a list of symbol libraries in the Library Explorer window and is mainly used to create new Symbol libraries, to copy/ move components to different symbol libraries. Also the symbol may be viewed using the Symbol Viewer.

Package Library

Displays a list of package libraries in the Library Explorer window and is mainly used to create new Package libraries, to copy/ move components to different package libraries. Also the package may be viewed using the Package Viewer.

Padstack Library

Displays a list of padstack libraries in the Library Explorer window and is mainly used to create new Padstack libraries, to copy/ move components to different padstack libraries. Also the package may be viewed using the Padstack Viewer.

Drag & Drop feature

- Select the component(s) displayed (using SHIFT or CTRL key).
- Click the left mouse button.
- Drag the mouse to Schematic or Layout editor.
- Release the mouse. The component(s) tags to the cursor with the  Relocate function tool enabled.
- Click the mouse left button to anchor the component(s) at the correct position.

Send to feature

1. Select the component(s) in the explorer.
2. Click the right mouse button. A menu pops up where select Send To-Layout/Schematic.
3. Now select the editor. The selected components are placed at the board datum (bottom left corner of the board).

Send To option will be enabled only if layout /Schematic Editor is open

Library Browser

Library Browser browses library elements (Parts/ Symbols/ Packages/ Padstack) from the available libraries (including Project library) included in the search sequence . The system will search for these components in the library and append to the search list. Apart from component name, various other information may be specified such as symbol name, package name, manufacture etc. to make the search easier. User has the possibility to use wildcard combination also.

Components in custom libraries will be listed only if they are included in the search sequence.

Starting Library Browser

1. Click on the option tool  to open Library Browser.
2. Select the library - All Libraries, Project Library (libraries loaded or present in the opened Project) or other libraries (e.g. other Libraries - 54TTL.PART)
3. Set the necessary options. Check All Conditions, to narrow the search taking into consideration all information entered for the options. If necessary check Match Case.
4. Click Find Now button. The system now searches the component(s) in the selected library with the options set and displays the result in the search list.
5. Select the component(s) from the search list and **drag & drop** into the Schematic / layout editor or **Send to Schematic/Layout.**

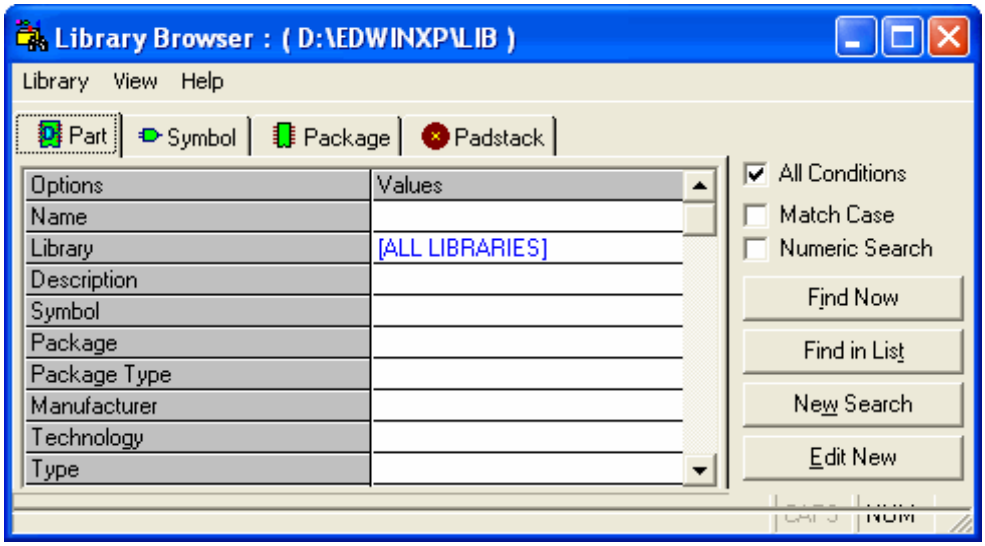


Fig.3.27 Library Browser

How to Add Components?

Components may be added to the current project without activating Library Browser/Explorer.

Components in the custom libraries will be pulled out only if they are placed higher up in the search sequence. Else they will be overridden by the first available component in the search list.

Steps:

i. Click on the option tool  Add components by name, from Add components to the circuit function tool of Schematic or layout Editor, to popup a textbox.

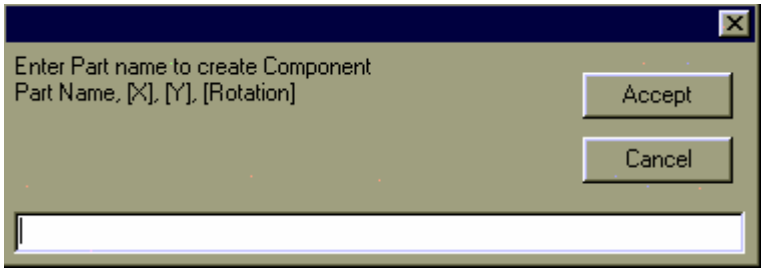


Fig.3.28

ii. Type in the name of the component to be added to the project.
iii. Click on Accept to get an image of the component tagged to the cursor.
iv. Click anywhere on the workspace to place it.

On each click on the workspace the component gets repeated until the Esc key is pressed. To position the component at a particular point on workspace, give the corresponding XY coordinate along with the component name.

EDSpice Symbol Editor

In order to simulate a schematic component using EDSpice Simulator, its symbol must be associated with one of the available EDSpice circuit elements or with the subcircuit from EDSpice Subcircuits Library. This application facilitates the association of symbols in Symbol library to the available EDSpice circuit elements or subcircuits and define the component parameters. EDSpice Simulation references may be added to parts or the already assigned ones may be changed using this module.

Starting EDSpice Symbol Editor

Click on the task *Library* in the Project Explorer and adopt either of the following methods:

- Right click on ***Library*** and then select the function ***EDSpice Symbol Library Editor***
- Select ***EDSpice Symbol Library Editor*** from the ***task list*** or from the ***task toolbar***.

The EDSpice Symbol Editor window opens as shown Fig.3.29.

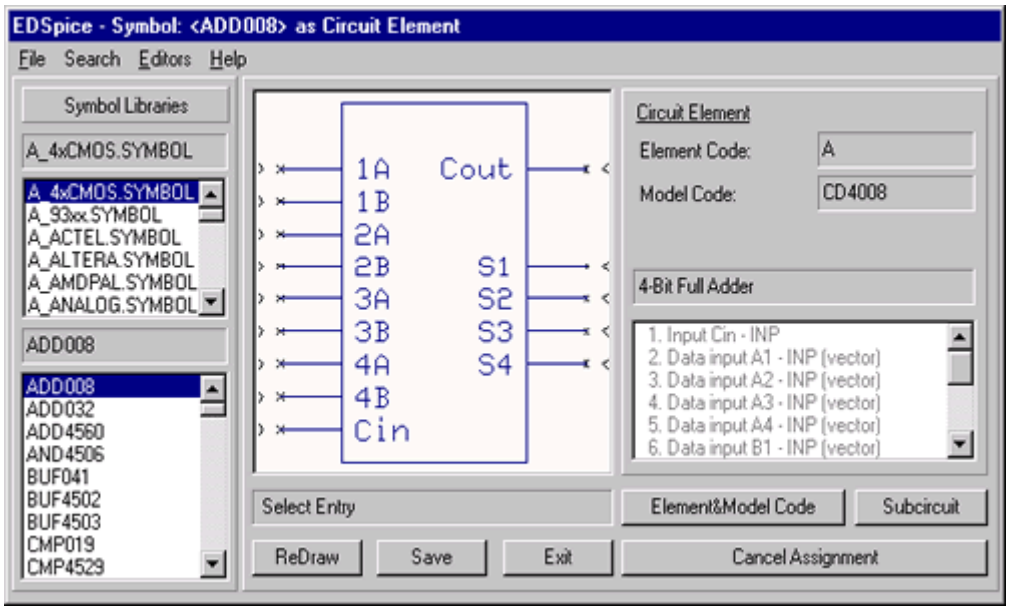


Fig.3.29 EDSpice Symbol Editor

 *The scale of the displayed symbol may be changed by pressing the hot key combination Shift U (Zoom Up) or Shift D (Zoom Down). The picture may be panned with center at current cursor position by clicking the right mouse button. The button when clicked redraws the symbol in current scale with entry #1 in the center of the picture.*

The required part/ symbol may be selected from their respective libraries or searched using the menu item *Search*. Either the part or the symbol may be searched according to the mode selected from the menu *Editors*.

Editors ➜ Symbol

The selected/searched symbol gets displayed in the display area. This symbol may be assigned element and model code or a subcircuit.

How to assign element and model code / subcircuit to the symbol

1. Select the appropriate circuit element from the list and press SUBCIRCUIT.

 *To assign subcircuit, if 'Add family prefix' is checked, the prefix gets added to the symbol.*

2. Assign element nodes to the appropriate entries of the symbol.
   When a circuit element has been selected, the list of nodes, as expected by EDSpice is displayed.
   The sequence of operations is as follows:
   - Position the cursor on the entry and click the mouse. The operation is confirmed if the selected entry is marked by a rectangle.
   - Select the appropriate node for this entry from the nodes list. The operation is confirmed if the entry is marked with the number of the node selected from the list.

   The same operation must be repeated for all entries in the symbol.

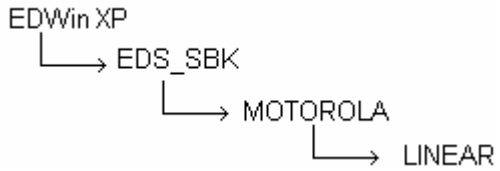
Editors➜ Part

The purpose of this mode is to set the Simulation Reference to the parts. In this mode, a new window overlaps the previous one and has two list boxes, one listing the part libraries in the selected library path and the other listing the parts in the selected *.PART library.

If the symbol associated with the part highlighted has a model code assigned to it, a list of model library names with the same prefix as the assigned one gets displayed in a list box to the right of the window. If the symbol has a subcircuit assigned to it, a list of library subcircuits with the same number of nodes as the assigned one is displayed.

EDSpice Simulation References are assigned to parts and not to symbols. Hence it should be noted that only those components created as parts would be properly attached to the subcircuit/ model parameters referred to by the Simulation Reference. The component has to be packaged before pre-processing by EDSpice.

While preprocessing the circuit in EDSpice simulator, the subcircuit/ (model code) assigned to the part overrides the default assignment made for the symbol. The specific subcircuit assignments made to symbols, if any, has the highest priority.



Users may create their own model/ subcircuit families and attach simulation reference to Parts adhering to the above mentioned regulations. Note that no subdirectory is allowed in the Model Parameter Library EDWinXP\EDS_MOD. Also, Family subdirectories for subcircuit should be of one level in EDWinXP\ EDS_SBK directory, e.g. the file structure shown in adjacent figure is invalid.

Field Editor

Field editor window lists all the components available in the Library. The main function of the utility is to maintain the existing libraries. Main purposes of this module are:

- To convert older libraries created in EDWin16 and EDWin32 to be compatible to EDWinXP format (Refer Chapter 2-Conversion Manager Page :39)
- Maintaining and updating the already existing libraries
- Creation of special parts
- Adding thermal parameters
- Upgrade old Package name to new Package name of a PART. E.g. DIP14 to DIP14/300. Here the physical attribute of the package is not affected.

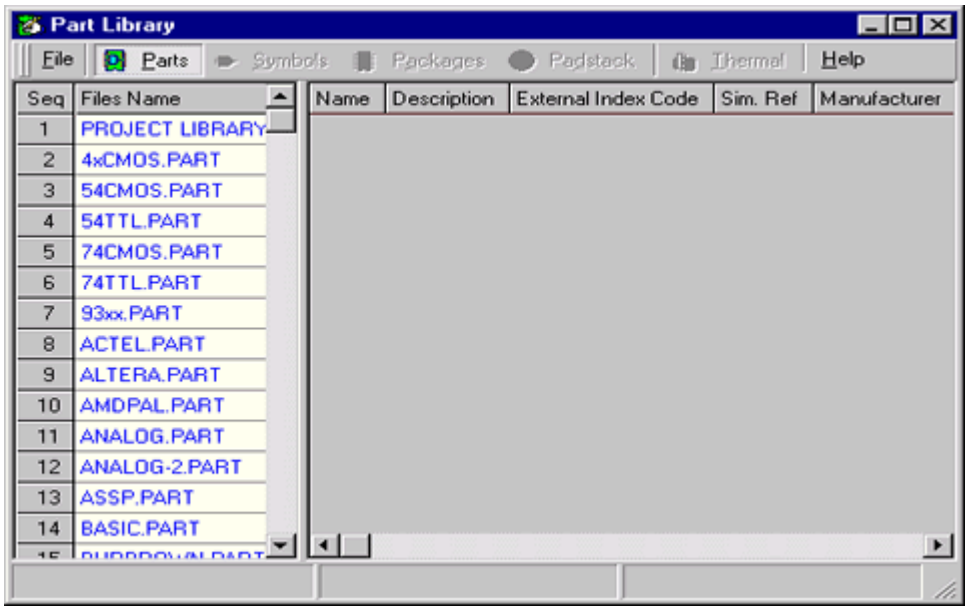


Fig.3.30 Field editor

Starting Field Editor:

This module may be invoked from Project Explorer in the following ways.

- Right click Library and select Field Editor from the list.
- Select Field Editor from the task list or from the task toolbar.

The window of Field editor is shown in Fig.3.30.

File

File menu provides a list of different library groups, each of which may be selected to obtain detailed information of components belonging to that category. There are options for setting the library path and refreshing the listed library on the left side pane.

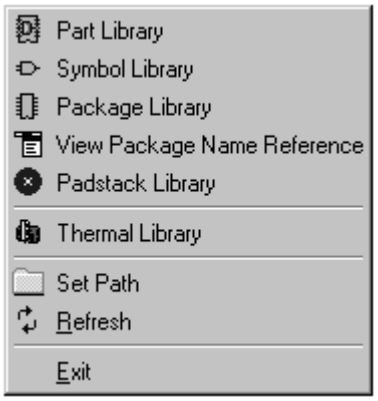


Fig.3.31

Parts

Selecting this option displays Field editor window with part tab activated. The window provides information about all parts available in the package. Details such as name, full name, External index code, simulation references, manufacturer, different types, technology, package type, simcode, element code/model or subcircuit/ variant, symbol name and package name of each of the parts are listed here. Double click on any of the listed part library on the left side pane to get property fields of different parts belonging to that group. Right clicking on any of its fields pops up a floating menu as shown below, this gives the option for updating the records, importing/saving it and for viewing separately the symbol and package. It also allows reading the system values of listed part fields.

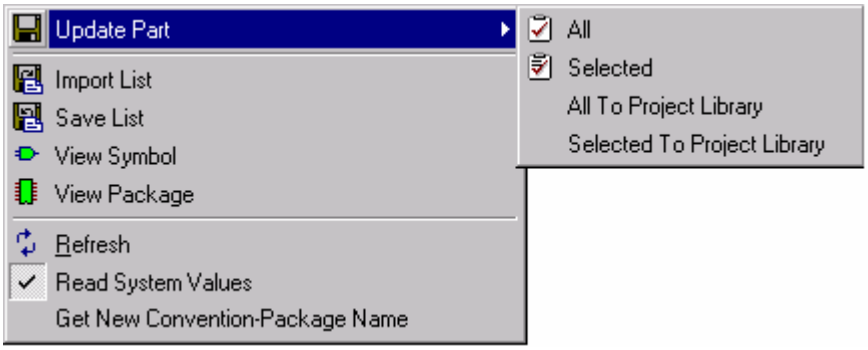


Fig.3.32

Update part All/Selected

Allows to update the records of either a selected part or all listed parts. Any modification done on this may be saved. Click on the required columns of any of the part's record for editing the values. User may either directly type in the values or it may be selected from a given browse list. Non editable fields are indicated by a light yellow color. If updating is tried on system libraries, the system issues an appropriate error message. Any custom libraries may be chosen for saving the updated information.

Import List

Allows loading *.DST files. Select this option to pop up a dialog box. On giving the necessary path the saved list gets imported.
*.DST files contain information of the parts saved previously.

Save List

Allows saving any of the listed part's fields information in the format (*.DST). Select this option to pop up a dialog box. On giving the necessary path the item gets saved as *.DST file.

View symbol

Using this option, symbol may be viewed separately in a viewer window.

View package

Using this option, package may be viewed separately in a viewer window.

Refresh

This option refreshes the displayed list of parts. If a record of any of the selected part is changed, the list on the right side pane will display the changed fields. Original fields (that which is stored in the system libraries) may be retrieved with this option.

Read System values

Selecting this option loads all the internal information about the part, which has been already specified. These system values cannot be changed. Disabling this option enhances the speed of loading libraries.

 *After enabling Read System values, it is necessary to Refresh the window.*

Get New Convention Package Name

When a Part library is selected from the Field editor window the package name displayed in the right side panel is the currently used name in the new version. But these names are slightly different from the convention names in the older version. Hence, for getting the old convention name corresponding to each package, this option has to be enabled. By selecting this option a window pops up displaying the packages not having their standard names. In the right side pane a new field displaying the old convention name will also be included. This option does not appear for Project Library as the physical attributes might be changed.

By selecting project library from the list, the right click pop up menu obtained will not be the same as above. It includes two more options as shown in Fig.3.32.

All to project library

By choosing this option all the listed component's field gets updated to the project library.

Selected to project library

This option allows to update only the selected part's field to the project library.

View symbol and view package (for the project library) options will only be active if there is the required information in the corresponding columns. By selecting any of the part, it's symbol and package may be viewed.

Symbol

Selecting this option displays Field editor window with Symbol tab activated. The window lists all the symbols available in the package. Double click on any of the listed symbol libraries in the left pane to get records of symbols belonging to that group. The different fields may be edited and the changed symbol record may be updated by selecting required options from the floating list obtained on right click.

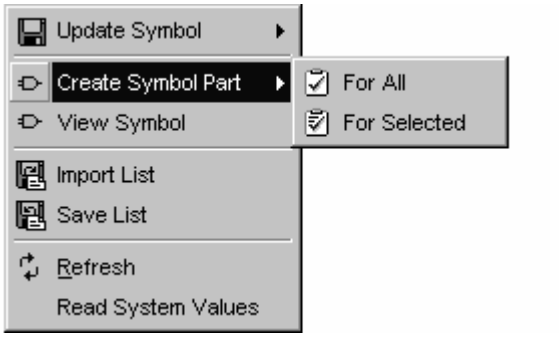


Fig.3.33

This module allows special creation of parts without an associated package. These are mainly used for simulation purposes. Right clicking on any of its listed records pops up a floating menu as shown below, which gives the option for updating the elements, importing/saving it and for viewing separately the symbol. It also allows reading the system values of listed items and refreshing the list.

Update symbols

Allows to update the records of either a selected symbol or all listed symbols. Any modification done on the listed fields may be saved using this. Click on the required columns for editing the fields. User may either directly type in the values or it may be selected from a given browse list Non editable properties are indicated by a light yellow color. If updating is tried on system libraries, the system issues an appropriate error message. Any custom libraries may be chosen for updating the symbols.

Create symbol part

Allows creating special parts without an associated package. Either a selected symbol or the whole list may be created like this special part. These are mainly used for simulation purposes. Selecting this option pops up a save dialog box in which a custom library may be chosen for saving the special parts. These special parts may be viewed by selecting the PART tab from the

main menu and double clicking on the required part library. The special part name has the prefix SMB_ added to the name of the original part.

View symbol

Using this option, symbol may be viewed separately in a viewer window.

Import List

Allows loading *.SST files. Select this option to pop up a dialog box. On giving the necessary path saved list gets loaded.
*.SST files contain information of the symbols saved previously.

Save List

Allows saving the listed symbol fields information in the *.SST format. Select this option to pop up a dialog box. On giving the necessary path the selected symbol library fields gets saved.

Refresh

This option refreshes the displayed list of items. If properties of any of the loaded items are changed, the list on the right side pane will display the changed properties. Original properties (that which is stored in the system libraries) may be retrieved with this option.

Read System values

Selecting this option loads all the internal information about the symbols which has been already specified. These system values cannot be changed. Disabling this option enhances the speed of loading libraries.

After enabling Read System values, it is necessary to Refresh the window.

Package

Selecting this option displays Field editor window with Package tab activated. The window lists all the packages available. Double click on the required package library in the left pane to get details of all packages belonging to that group. The different parameter fields may be edited and the changed package record can be updated by selecting required options from the floating list obtained on right click.

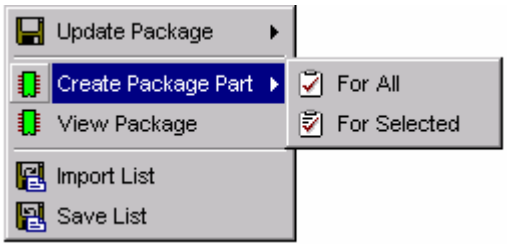


Fig.3.34

This module allows special creation of parts without an associated symbol. There are options for viewing the packages separately and for importing/ saving it. Pop up list obtained on right click is as shown in Fig.3.34.

Update package

Allows to update either a selected package field or fields of all the listed packages in the selected library. Any modification done on the listed property

fields may be saved using this. Click on the required columns for editing the values. User may either directly type in the values or it may be selected from

a given browse list. If updating is tried on system libraries, the system issues an appropriate error message. By this users are prevented from tampering the system libraries. Any custom libraries may be chosen for updating the packages.

Create package part

This option allows special creation of parts without an associated symbol. This is mainly be used for creating mounting devices. Selecting this option pops up a save dialog box in which a custom library may be chosen for saving the special
parts. These special parts may be viewed by selecting the PART tab from the main menu and double clicking on the required part library. The special part name has the prefix PKG_ added to the name of the original part.

View package

Using this option, package of the selected part may be viewed separately in a viewer window.

Import List

Allows loading *.LST files. Select this option to popup a window, in which the required path may be browsed to import that item.*.LST files contain information of the package saved previously.

Save List

Allows saving the listed Package fields information in the *.LST extension. Select this option to popup a dialog box and enter the required path to save the list.

View Package name reference

Selecting this option opens a window "Info", which displays the names of the packages in accordance with the old and new conventions. Corresponding to each old convention package name, the new name is displayed. .

Padstack

Selecting this option displays Field editor window with padstack tab activated. The window lists all the padstacks available. Double click required padstack library in the left pane to get details of padstacks belonging to that group. The different parameter fields may be edited and the changed padstack record may be updated by selecting required options either from the main menu or from the floating list obtained on right click. There are also options for viewing padstacks separately and importing/saving it.

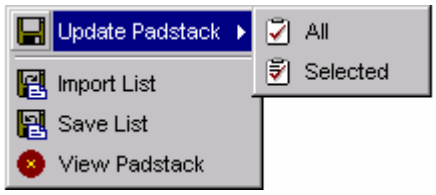


Fig.3.35

Update padstack

Allows to update either a selected padstack field or fields of all the listed padstacks. Any modification done on the listed property fields may be saved using this. Click on the required columns for editing the values. User may either directly type in the values or it may be selected from a given browse list. If updating is tried on system libraries, the system issues an appropriate error message. Any custom libraries may be chosen for updating the fields.

Import list

Allows importing *.PST files. Select this option to pop up a window in which the required path may be entered for loading the saved list.*.PST files contain information of the padstack saved previously.

Padstack Save list

Allows saving the listed Padstack fields information in the *.PST extension. Select this option to popup a window. Enter the required path. The list is saved in that location.

View padstack

Allows viewing pads in a separate viewer window

Thermal parameters

Selecting this option displays Field editor window with thermal tab activated. The window lists all thermal libraries available. The different fields of thermal parameters may be re-edited from this window. The changes may be saved in a custom library other than the system libraries. If modification is attempted on the existing system libraries, the system will issue an appropriate error message. Double click on any of the listed thermal libraries to display the corresponding thermal parameters associated with each component. Right clicking on any of the listed component in the right pane pops up a list that allows to update, save and load items. This pop up list is shown in Fig.3.36.

Fig.3.36

Update Thermal Values

Any of the listed component's thermal parameter fields may be edited by clicking on the corresponding columns. User may either directly type in the values or it may be selected from a given browse list. These changed fields may be updated by selecting this option. Updating of the changed fields may

done on any of the custom libraries other than the system library. If updating is tried on system libraries, the system issues an appropriate error message.

There is option for updating either a selected or all the listed component thermal parameter fields.

Import list

Allows loading the *.DAT files. Select this option to pop up a dialog box in which required path may be given for loading the saved list.

Save list

Allows saving the selected component's thermal fields in the ` *.DAT format.

Set path
Allows to set the path of required libraries.

Refresh.
This option refreshes the listed libraries by reloading it from the disk.

Exit
Allows to exit from this module.

☛How to pass older (EDWin 16 and EDWin32) library components through Field editor?

1. Using Conversion manager convert EDWin 16 bit libraries. EDWin32 libraries need not be converted.
2. Open Field editor, and choose the path where library is residing.
3. Double click on the required library and on right pane, right click and enable option Read System Values and Refresh.
4. Now these libraries may be added with required information and updated.

☛How to Import older libraries and databases (projects)?

- **Using EDWin 16 libraries and databases.**

All EDWin 16 bit databases and libraries should be converted to the new format using Conversion Manager (exactly as in EDWin 32).

A library element in the new format contains additional fields for storing cross-references and in case of parts even thermal parameters These cross-references are not needed for proper functioning of the system but are useful for searching and browsing. Since this information cannot be reconstructed automatically during conversion, a special program called Field Editor has been provided. Certain cross references required for proper functioning of Library Browser and Library Explorer will be updated automatically when library file is passed through Field Editor. For example: in EDWin 16 thermal parameters were kept in separate files (.DAT/ .TAL). Now all this data is stored within the respective Parts. Field Editor also enables to add other necessary information (manufacturer name, type etc) in manual edit mode.

In the latest version, when you try to save old DEVICES or PARTS taken from old DATABASES, it is required that you have to save the corresponding symbols and packages used by the Parts into User Libraries (and of course subsequently included those files into the Search Sequence).

- **Using EDWin 32 Libraries and databases.**

All EDWin 32 libraries and databases are upward compatible and for viewing with the latest version NEED NOT be converted.

Although, for using the libraries, it is required to pass the library files through Field Editor.
CAUTION:

Any attempt (even for browsing using Library Explorer or Browser) to access EDWin32 libraries from the latest version causes permanent change of format. EDWin 32 libraries and databases once used with the new package cannot be used with EDWin32.

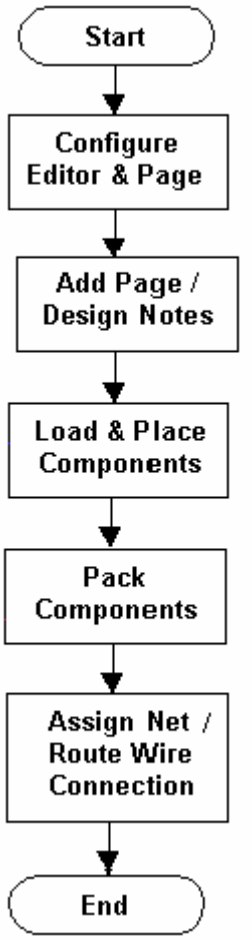
PLEASE ALWAYS USE SEPARATE COPIES OF LIBRARY AND DATABASE FILES FOR EDWIN 32 AND NEW VERSION.
THE PATHS FOR LIBRARY AND DATABASE FILES OF EDWIN 32 AND THE NEW VERSION MUST NOT BE SAME...

In the latest version, when you try to save old DEVICES or PARTS taken from old DATABASES, it is required that you have to save the corresponding symbols and packages used by the Parts into User Libraries (and of course subsequently included those files into the Search Sequence).

Chapter 4

Schematic Editor

The Schematic Circuit Diagram is created in the *Schematic Editor*. The circuit thus captured is automatically front-annotated to the Layout mode on packaging.
It provides the facility to perform both manual and automatic operations. It also provides tools to add text information to the circuit, thereby increasing its readability. The flowchart outlines the process of Schematic Capture.



Configuring the Editor

The first step in creating a Schematic is to set the working environment. There are different settings to be made before working on a project. Global settings for working with the system are made in Project Explorer | System | Options. However if a user would like to make exclusive settings for the current project, Project Explorer |

Project | Project Options Setup may be used. An example of a global setting is the **Library Path**. This instructs the system where to find the Library components.

Library Path

During installation, system libraries are placed in DRIVE: \EDWinXP\Lib. The user can also set the working directory for the library files in the following way:

- Project Explorer | right click on System.
- Select Options. The Options setup dialog pops up.
- From the options list, select Files | Folders.
- Set the path by clicking on the corresponding grid cell.

Menu

Tools

Displays a list of menu items that is present in Schematic, Layout and Fabrication Manager. The menu in this list differ in each editors and when selected allows entering into main object oriented function.

Tools (Components)

Enters into component editing mode presenting various tools that performs operation related only to components.

Tools (Connections)

Enters into an editing mode, which presents various tools that performs operation related only to the connection between components.

Tools (Page Notes)

Enters into an editing mode, which presents various tools that performs operation related to Notes and Graphics on the Schematic individual Pages.

Tools (Block Edit)

Enters into block editing mode presenting various tools that performs operation related to objects like components/ wires in block.

Tools (Autoplace)

The tools required to auto place components is displayed automatically on the workspace when Tools | Autoplace menu is invoked.

Tools (Page Format)

Enters into page editing mode presenting various tools that performs operation related to editing the default page format.

Tools (Design Notes)

Enters into design notes editing mode presenting various tools that performs operation related to Design notes.

Tools (Bitmaps)

Enters into bitmap editing mode presenting various tools that performs operation related to bitmaps.

Tools (Convert truth table to diagram)

Enables conversion of truth table to schematic diagram.

Tools (Convert VHDL Code to diagram)
Enables conversion of VHDL code to schematic diagram.

Tools (Filter Designer)
Enables filter designer to design different types of Active filters by entering specifications. This will generate Filter circuits in the schematic editor, which can be used as part of other circuits.

Preferences
Provides a dropdown menu, which may be selected/ deselected to set various features. These features directly affect the working environment.

Enable undo/ redo:
If this option is unchecked undo and redo options under edit menu remains disabled. This option provides a faster working environment. Activating/ deactivating this option in Schematic automatically enable/ disable the operation in Layout and vice versa.

 *In the Options window (Project Explorer | System | Options) there is an option for selecting the number of steps for performing the Undo operation. Increase in the number of steps reduces the system speed.*

Zoom factor:
Opens an input box that allows specifying the zoom factor. This factor determines the next zoom level when zoom operation is performed or more appropriately, the current zoom precision is increased/ decreased by this zoom factor.

Calibrate Ruler:
Allows calibration of the ruler according to user's need. Workspace settings allow selecting one of four ruler calibration modes.

Operation
Auto: Here the calibration factor will be automatically adjusted to scaling factor (usually in multiples of 2, 5, and 10). By selecting this option the minimum scale value that can be displayed by the ruler adjusts automatically to current precision resulting from zoom up/down operations.
Fixed: By selecting this option ruler will be calibrated in multiples of 10.

Grid: By selecting this option, the ruler will always be scaled as a multiple of the selected grid value. When zoom precision is increased or decreased the grid value may be changed. But the calibration factor will always be the initially selected grid value.

Custom: Selecting this option displays a text box in which calibration factor for scaling the ruler may be entered in the range 1-10. The ruler displayed will always be a multiple of the value given in the text box.

Customize toolbar:
Opens Customize toolbox where users are allowed to select the most commonly used function tools from Schematic editor and arrange them in custom toolbox. The purpose of this custom toolbox is to provide direct access to object oriented function

tools, bypassing selection of function tools from different modes (component, wires). I.e. a collection of function tools of different modes may be customized to form a Custom toolbar. Skilled users especially prefer this toolbar.

Mixed Mode Simulator:
This option allows the user to switch from Schematic Editor to Mixed Mode Simulator. The Mixed Mode Simulator is EDWinXP's native simulator and provides facilities to simulate and verify the circuit using various analyses.

EDSpice Simulator:
This option allows the user to switch from Schematic Editor to EDSpice Simulator in the application. This simulator is a plug-in extension of EDWinXP and runs various analyses on the circuit based on SPICE conventions.

Instant Net Name:
Usually when a wire connection is created, system assigns the first free number to the nets. But when this option is enabled, system allows to predefine the net name according to your choice.

Select this menu item from Preferences. Using the Tools | Wires toolbar, start a wire connection. System instantly pops a window where the name may be specified. Now every time a new wire/ trace is routed, an input box pops up where the name for the new net may be entered. If this option is disabled, system automatically assigns net name (UN1, UN2…) to the newly made connection.

Instant Wire Label:
If this option is enabled, default net label may be obtained at the time of wire creation. Enable this option by choosing it from Preferences | Instant Wire Label. On creating a new trace its default name will get tagged to the cursor. Click anywhere on the workspace to place the label.

Instant Packaging:
Allows to package components as soon as they are loaded into the workspace. All the constituent groups of the part will be loaded. This is particularly useful while loading connectors into the Schematic.

Guidelines (Net):
Allows displaying a single ratsnest associated with the selected net while routing or relocating a wire/ trace.

Select this menu item from Preference and click on any node. The entire nodes associated with that net is displayed as ratsnest. This feature is particularly useful when the layout is prepared first.

Guidelines (Next Unconnected Node):
Allows displaying the next unconnected node associated with the net while routing or editing.

Select this menu item and click on any of the node. The next nearest node associated with the net is displayed on the page. Take the connection to that node.

Similarly all node of that net may be connected using wire. This feature is particularly useful when the layout is prepared first.

Delete Unnamed Nets When Connection Deleted:
This option when enabled, deletes the whole net when the wire connection is deleted, provided the net is not named.

Horizontal Net /Bus page links:
This option when enabled, displays net/bus page links horizontally.

T-connect Same Net Only:
Allows T connections to be made only if they are of the same net.

Autoroute "to Pin" connections:
Auto-connector automatically routs last wire segment if the segment is connected to component pin. When pin-to-pin option is set then every connection is routed. Auto-connection is disabled when "Option to route only orthogonal connection segments" is ON or if Preference "Autoroute "to-pin" connections" is OFF.

Reroute component connections after Move:
The option serves an important purpose of automatic reconnect the nodes of a component if the component is relocated or swapped.

X/Y Coords:
Allows determining the current cursor position with respect to a given reference point in terms of the X and Y coordinates/ distance. The values are displayed in the position toolbar.

This menu item comes under the Preferences menu. When enabled, the X and Y coordinates/ distance values is displayed in the status bar with respect to a given reference position. The options X/Y Coords and Distance toggles between one another. X/Y Coords is the default option.

Center:
This menu item comes under the Preferences menu and allows setting the origin coordinates to the Center. The co-ordinate information displayed in the position toolbar is with reference to a point on the page. This defines the center of the page as reference point for all coordinate and dimension information.

Format Datum:
Allows setting the origin coordinates to bottom left corner of the page. The origin coordinates (0, 0) is now marked at the bottom left corner of the page, which is set as the reference point.

Refpoint: Allows setting the position of the origin coordinates on the workspace with respect to a reference.

Lock Toolbar: Anchors all the toolbars at the placed location.

Info

The items in this menu provide information about the various objects/items created on the schematic diagram. It allows assessing free symbols, parts, packages, number of nets, etc. The necessary information is displayed in the respective info window.

General

Opens a dialog box where general information regarding the objects placed on the workspace may be obtained. Double clicking the particular object in this dialog highlights the particular object on the workspace. This menu may also be invoked by using shortcut CTRL+F. This dialog may also be used to find particular object on the workspace. There is a slot for Find operation in each tab of this window. In order to find a particular item, select the tab corresponding to the type of object/ item to be searched. Type few characters of the item or select the item from the drop down list. The objects along with corresponding details are viewed in the selected tab. Now click on the particular object/ item on the right side to highlight the selected item/ object on the workspace. Following are the object information's that can be obtained.

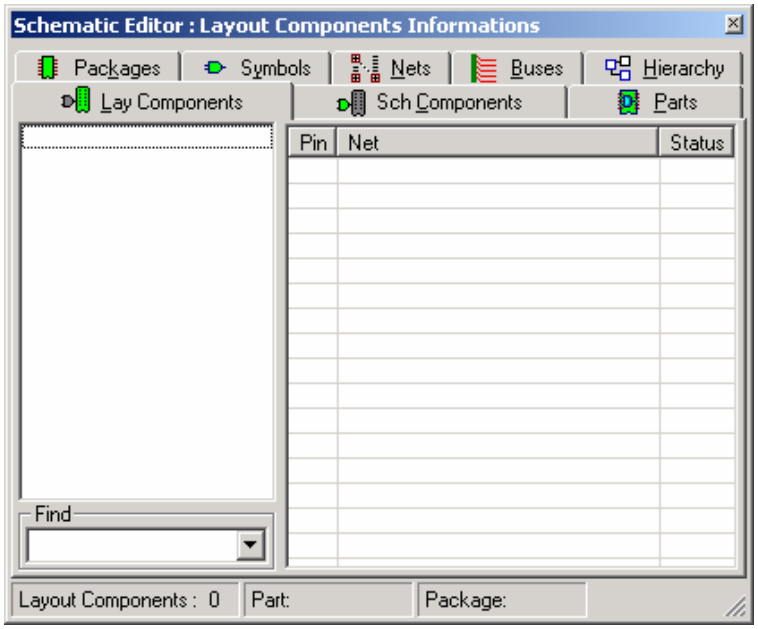


Fig.4. 1

Layout components information: Displays Layout component information window where the layout components used in the current project is listed

Schematic components information: Displays Schematic component information window where the schematic component used in the current project is listed

Parts information: Pops up a window Part Information displaying the list of parts used in the current project (database) and information associated with

each part. For EDSpice Simulator, the corresponding window shows the elements currently in use, its status and EDSpice reference ID details.

Packages information: Pops up Package Information window displaying the list of packages used in the current project (database).

Symbols information: Pops up a window Symbol Information displaying the list of symbols used in the current project (database).

Nets Info: Opens a window Net Information that displays information of all nets present in the current project (database).

Buses Info: Opens Bus Information dialog box that provides general information about the buses used in the project (database).

Hierarchy Stack

Opens a window to display information on the current hierarchy and the hierarchy from which the components of the present hierarchy is generated. This menu item may be selected either from General tab window or from Info menu to pop up a window "Hierarchy structure". Both the dialogs provide details such as name of the current hierarchy used. If the components of the pertaining hierarchy have been generated from other hierarchies, all information regarding the original hierarchies is displayed. The Info window displays only the current hierarchy if the existing hierarchy is not generated from any other hierarchies.

General Settings

Relevant settings of Schematic Editor can be made from the Preferences menu. The following settings may be made in the beginning

1. Enable Undo and Redo – enable this menu to enable Undo and Redo operations. The recommended setting is ON. Turning this OFF will make the system faster.
2. Zoom factor – Pressing the '+' key increases the zoom by a value which is determined by the value of Zoom factor. The default value is 2, i.e. each time the + or – key is pressed, the workspace will be zoomed to double the current value of zoom precision. For smaller changes in magnification on pressing the Zoom buttons, set the value as 1.1.
3. Instant net name – by default when a wire is created, the system allots it a net name UN1, which is by default an Unnamed Net. Enabling this menu will cause an input box to be displayed each time a new net is created so that the user can specify the name of the net. For the purposes of simulation and display of results it is always better to keep meaningful net names. This feature will eliminate the need of renaming most nets.
4. Instant wire label – enabling this option will automatically cause a label to be placed each time a new wire is created. The label will be the name of the net.
5. Guidelines (Next Unconnected Node) – displays a rubber band connection to the next unconnected node in the selected net. This can be turned ON while routing.

The above option is relevant only in situations where nets are already assigned. This is particularly useful for placing and routing projects imported from SPICE netlists, VHDL etc.

The Grid value can be set to 0.1000”

The Snap value can be set to 0.0500”. For making fine movements, the snap value can be decreased.

It would also be a good idea to enable the following toolbars from the View | Toolbars menu – Function tools, Option tools, Tools, Standard, Sizes, Position and Schematic View.

Page Configuration

Before capturing the actual circuit, it is advisable to set the required page size to avoid unnecessary wastage of space. On invoking Schematic Editor page, although a default page outline is provided, user can select pre-defined formats or create own formats.

Features

- Maximum page size available - 4m x 4m.
- Maximum number of circuits /Hierarchies - 99
- Maximum number of pages in a circuit – 99.
- Available page formats – American & European.

American formats: A (landscape), B, C, D, E, A (portrait)

European formats: A4 (landscape), A3, A2, A1, A0, A4 (portrait)

By default American format A (landscape) is enabled.

Steps to follow

How to set page format?

Edit page format

i. Select  Redraw | Page from Standard Toolbar to display the default page within the GUI window as shown in Fig.4.2.

ii. To place objects on the page, you may select an object and simply position wherever required. However, you can exactly position components by enabling  Ruler from Schematic view toolbar. Ruler gets aligned to the sides of the page as shown in Fig.4.1 and remains displayed until it is disabled. By default, ruler is displayed.

iii. Use the function and Option Tools provided to edit the page outline.

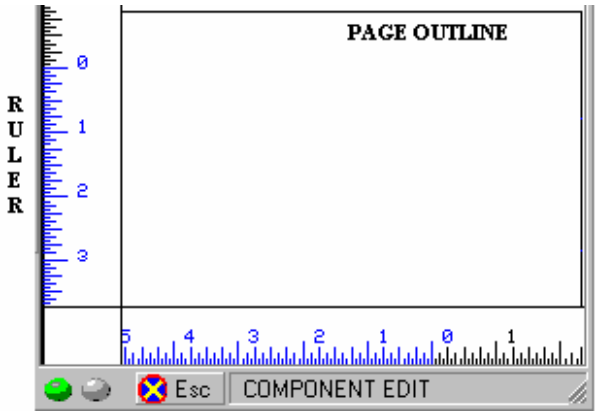


Fig.4.2

How to define page format?

i. Select  Page Format from Tools toolbar as shown in Fig.4.3. The tools in the

ii. Function and Option Toolbar changes simultaneously.

Fig. 4.3

iii. Select  Define Page Function Tool (by default appears selected). The Page format window appears as shown in Fig.4.4:

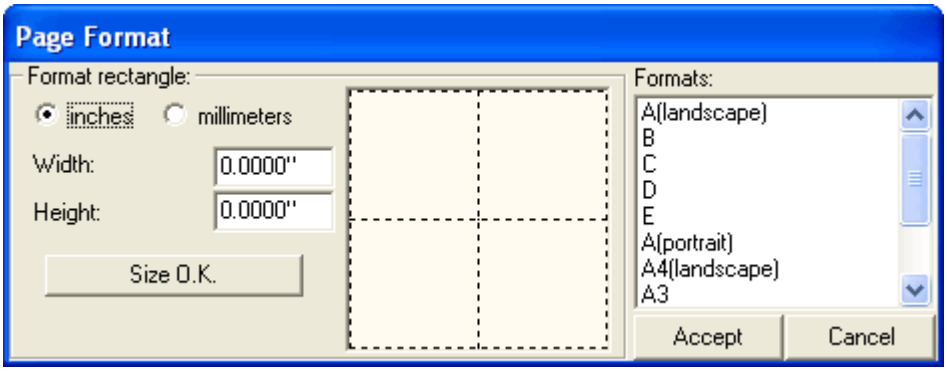


Fig 4.4

iv. The page format may be defined by either of the following two ways.

v. Select standard formats (e.g. A4 (landscape)) from the list.

vi. Enter the required height and width in the text box provided and press SIZE OK.

vii. In either of the two options selected, a miniature representation of the page format is displayed in the picture box provided.

viii. Now click on ACCEPT button to reflect the selection.

ix. Select  Redraw | Page from the Tools toolbar to display the default page within the GUI window.

Schematic Capture

Double click on the task 

in the Project Explorer to open Schematic Editor. This tutorial will discuss the creation of the Schematic Diagram of Half Adder (Refer Fig. 4.5).

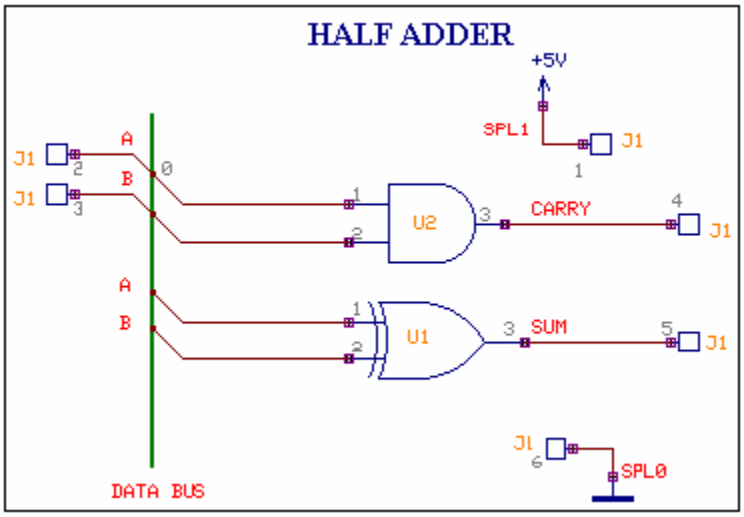


Fig. 4.5

Loading the Components

Before we start loading components on the page, turn ON Grid 3(Grid is the dot raster which when enabled, helps in assessing position and distance while placing graphical item(s)) by enabling the grid from the dropdown,  in Standard Toolbar. The value for grid may be selected from the drop down list as .1000". Similarly, set Snap value to .0500" for better placement of the components.

[3] Grid is the dot raster which when enabled, helps in assessing position and distance while placing graphical item(s)

Select  Components from Tools toolbar and right click on the workspace to popup a set of Component editing tools. By default,  Relocate tool is enabled.

Creating circuit diagram of HALF ADDER:

1. Right click in the workspace and select  Add Components to the Circuit, now click on the option tool  Add Components by name from the popup menu. This opens up an input box, enter 7408, (the Part name[4] of AND gate) and click the ACCEPT button to return to the workspace with the component attached to your cursor. Click on the workspace to place it. A copy of the component is still attached to the cursor, so that the component may be repeated. Since only one instance is required, press ESC. A-label is attached to the components placed indicating the component name. In the same way load 7486. Steps 2) 3) and 4) describe another method of loading components.

 *Selecting*  *Add Components by name tool and specifying the X, Y position together with the angle of rotation will place a single component at the exact location.*

You may also load components from **Library Browser** which provides options for multiple loading of components, searching for a component, viewing the details of components, etc.

2. To load 7408 from Library Browser, right click and select  **Add Components** to the Circuit and then click on the option tool  **Browser to add components** tool. Select Parts tab from Library Browser window that appears. Type 7408 in the Name field. Select 74TTL.PART from the drop down of Library field and click ***FIND NOW***. The search results will be listed below.

   Drag the item in the list and Drop it on to the Schematic (or right click on the selected items and press Send to / Schematic). Setting all options provided in Library Browser narrows search. For more details on Library Browser, please refer EDWinXP Help. In the same way search for7486. Now the list contains 7408 and 7486. Multi- select both by pressing the SHIFT/CTRL key. Right click, to popup a menu.

[4] **Part Name** is the name by which a component is available in the market , it is also called **ordering information** In EDWinXP components are loaded with their Part names rather than the symbol names like INV, 2NAND etc

Select **Send to / Schematic**. You will find the Parts placed at X, Y (0, 0) location (by default it is at page datum) in the Schematic. The selected components may also be dragged and dropped to the workspace. If one is not familiar with Part names, select **Symbol tab**, enter the symbol name, i.e. 2AND, and press Find Now. A list of symbols with the name 2AND appears. Right click on one symbol and select Used by Part / ALL LIBRARIES. A list of parts using the symbol appears; load any on the Schematic using the methods described above.

3. Another method of loading components is by using the Library Explorer, which can be launched by, right click in the Schematic Editor -> **Add Components to the Circuit,** select the submenu **Explorer to add components**. This is similar to Windows Explorer and it shows all the libraries available in the default Library path. Select the library, 74TTL.PART and select the parts 7408 and 7486 (press Ctrl key and select with left mouse click) and load into the workspace by Drag drop / Send to menu in the right click popup menu.

4. Another method of loading components is by using the component browser, which can be launched from View->Schematic->Browser (Refer Fig. 4.6). The required components can be obtained either by using the Browse option in the window or by Search for the element in the quick menu. Once the element is found, it can be placed in the workspace using the Place button in the bin. Hotkeys can also be assigned to element names by which quick launch of components is possible.

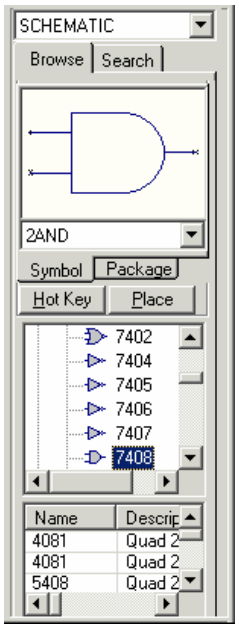


Fig. 4.6

5. Half adder needs to make connections to a voltage source, Ground and signal generators for the two inputs. These are external sources (which will not be housed on the PCB) and hence connections to them can be shown with the help of connectors. Take Library Browser to get the pop up window as shown in Fig. 4.7 and type '* 'in the Name field and '*connector*' in the Description field as shown below and press Find Now. The Library Browser will display all the components in the Library with the word connector in its Description (which is entered at the time of Part creation). In the list of parts that appear, select LIST6 since we 6 input output connections.

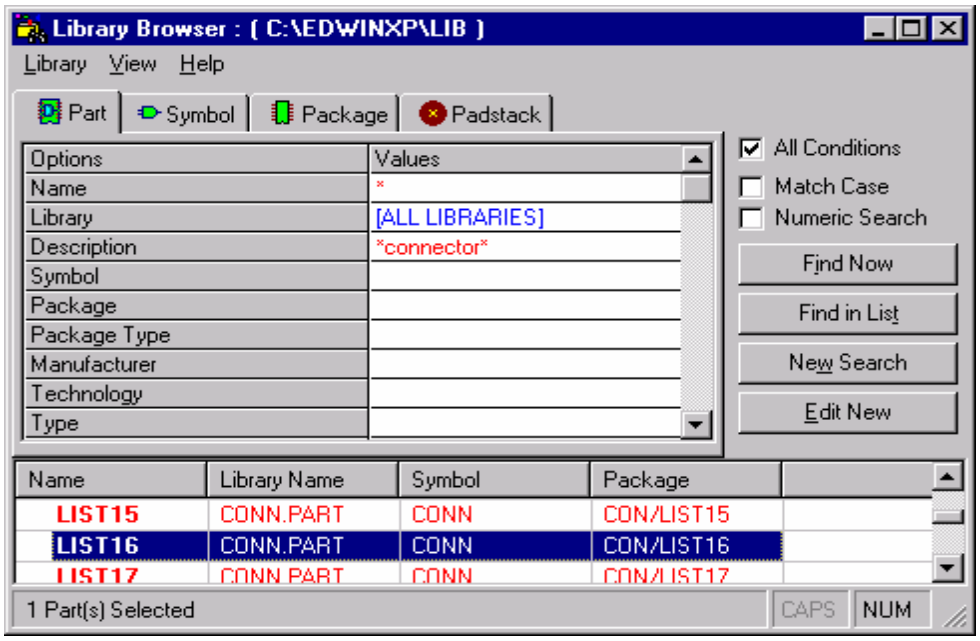


Fig. 4.7

Load the connector and using **Repeat Component** function tool, create 5 more instances. Similarly load SPL0 (Hotkey G) and SPL1 by typing these names in Function tool **Add Components to the Circuit** and its option tool **Add components by name (F3).**

6. To relocate the component, right click[5] and select tool Relocate. Position the part where required and click the mouse to place component. When you relocate a component from a cluster of components, all other components present may disappear. Clicking Redraw tool brings the components in view again. The component entries must be placed on the grid for effective wiring. Proper selection of Grid and Snap value is a must.

Tip

a) Components may be relocated using bullets. To select (bullet) a component, press Ctrl key and click on the component. Bullet gets placed on the component and its function is Relocation. Move the mouse over the bullet. Now the mouse pointer will change to move pointer. Click on the bullet and drag to required position.

b) You may use Shift + Z to get a full screen cursor that aligns the symbol on workspace while any operation such as relocation, repeat is performed.

c) Pressing the SHIFT key while relocating/ stretching an item, overrides snap value set allowing the item to move/ stretch smoothly.

[5] Instead of using Right click menu for selecting function tools, they may also be activated from their toolbars which are by default placed on the left of the workspace. These toolbars are dock able, i.e. they may be relocated and placed anywhere on the editor window. To lock toolbar position select *Preferences / Lock toolbar* (**CTRL + H**)

7. With the Function tool  **Relocate** selected, click on 7408 to select it. The AND gate gets highlighted, now move the cursor and press left mouse button (or SHIFT + ENTER) to fix the component at that location. Repeat the same procedure with 7486.
The Parts are placed as shown in Fig. 4.8. The connectors have been placed in such a way that the end pins, 1 and 6 are devoted for Power/Ground signals. On packing the pin number to which the entry corresponds to will appear (refer the picture, all the numbers in grey are the corresponding pin numbers in the package).

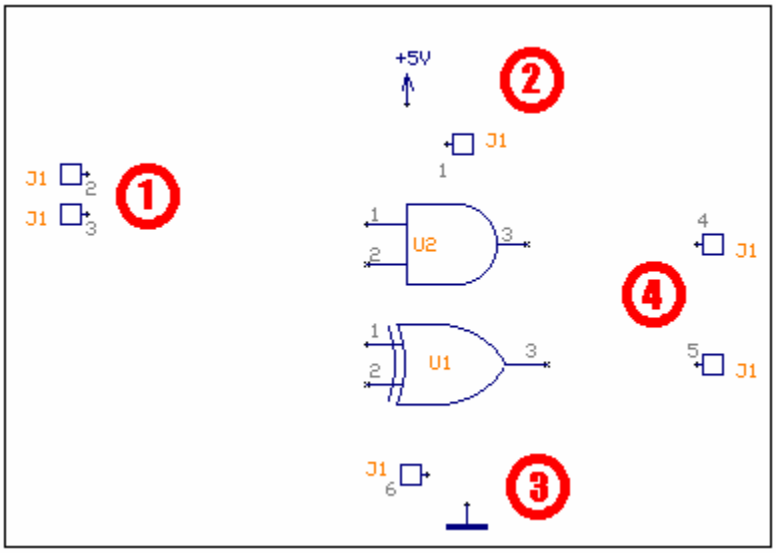


Fig. 4.8

Half adder has six different signals, i.e., A,B,SUM,CARRY,Vcc and GND. In EDWin XP common terminology for Vcc (+5V) is SPL1 and GND is SPL0. The printed circuit board requires connections to signal generators for A and B, these can be made by connectors shown near .location marked 1 in the picture above,
location marked 2 is for making connections to SPL1, 3 for SPL0 and 4 for output connections (for signals SUM and CARRY).

 *Please refer EDWinXP / Help / Show me How / Schematic Editor / Component editing tools to view movies illustrating the methods described. Make sure the EDWinXP CDROM is inserted in the CD drive.*

Autoplacing the Components

In case of complex circuits you can use the tool  **Auto Placer** for automatically placing the component in the workspace. The Auotplacer provide different function as well as option tools for the easy placement of components . Autoplacer can do the following:

a. It can automatically place all components outside of the page boundaries and sort them according to parts.

b. It allows user to relocate single components and manually place them according to selected placement cell patterns.
c. It allows user to identify other components connected to selected component on the page and manually place them according to selected placement cell patterns.
d. It allows to automatically place components connected to selected one.
e. It allows to automatically place all connected components starting with those connected to selected component.
f. It allows to build groups of components and relocate these groups to desired position on the page.
g. It allows to automatically build new groups of components using the currently present group as template and relocate this newly created group to desired position on the page.

Packing the Components

If the PCB of the circuit has to be designed, then the components need to be packed. Packaging is nothing but information that the system requires to identify the Package, associated to Part placed on the Schematic. For example, symbol 7408 is associated to package DIP14 in layout. Only packed components are ***front annotated***[6] to layout.

EDWinXP supports three types of packing.

Autopackaging

Select **Tools | Component |**  **Pack/Unpack Component** and select  **Autopackaging** from the option list. An Automatic Packaging window appears as shown in Fig. 4.9. Click ***Execute*** button. The packaging information appears along with each of the packed components. Automatic packaging assigns first free number to the last placed component belonging to the same group.7

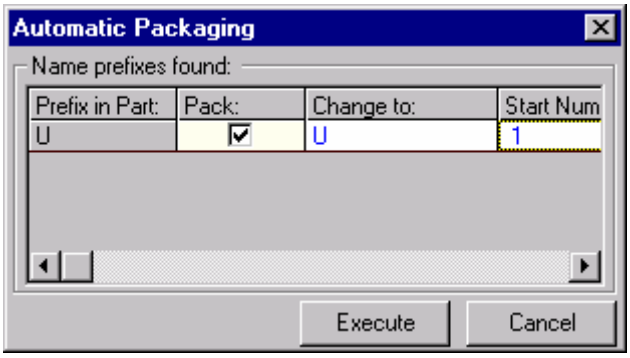


Fig. 4.9

[6] Automatic update of PCB Layout with changes are made in Schematic. Conversely ***Back annotation*** refers to automatic update of Schematic with changes made in PCB Layout.
[7] **7404** has six **INV** gates, each gate is referred to as a ***group***. Parts which have the same kind of groups are called **Homogeneous** Parts while Parts like **4000** which have different groups (**3NOR** and **INV**)are called **Heterogeneous** Parts.

Instant Packaging

Instant packaging is invoked using the tool under **Preferences** menu in **Schematic Editor →Instant Packaging** which helps to pack components as soon as they are loaded to the workspace. All the constituent groups of the part will be loaded. This is particularly useful while loading connectors into the Schematic.

Interactive Packaging

Interactive packaging is done using the tool  **Pack / Unpack Component**. Right click and select this tool and click on the component pin that is to be packed. A window **"Component Packaging"** pops up (Fig. 4.10). Click ***ACCEPT*** button. This method allows individual packaging of components.

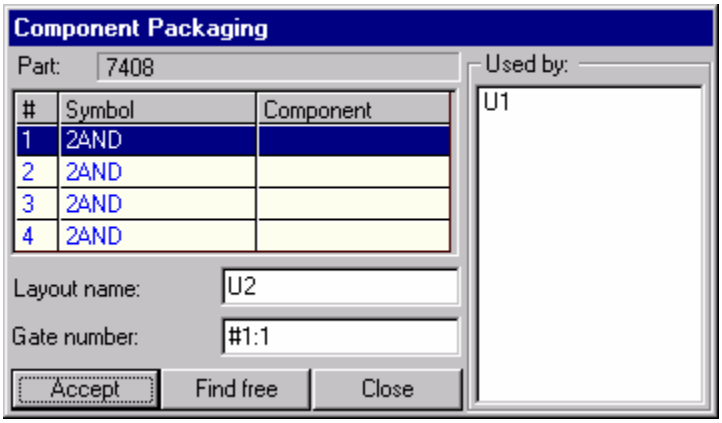


Fig.4.10

Packaging Using Property Window

Packaging can also be done using the property window. This is a form of manual packing, as the user has to select the component (CTRL + Click) to be packed and activate the property window of that component. The steps are as follows for packing component by component:-

1. Select the component by bulleting (CTRL+Click).

2. Right click and select properties to get the Property Sch Component window pops up.

3. In the property window right click on the component and use pack option.

The steps to pack all the components at one instant:-

1. Select Info->General or Ctrl + F
2. Multiple select the components (Schematic component).
3. Right click and select properties to get the Property Sch Component window pops up.

4. In the property window right click on the schematic component and use pack option.

Establishing Connections for the Circuit

Connections between components are established using **WIRES** and **BUSES**.

Select  **Connections** from **Tools** toolbar to enable a set of tools required for routing.

Tip: Adjust zoom precision to view the terminals being wired. Turn ON grid and snap to help in positioning the wires.

1. Creating the data bus

Select the second Function tool  **Create Bus**, click on the workspace and drag the cursor and left click when the bus has the required length, right click and press  **End Bus**. An input box appears, enter a name for the bus, say Data bus.

The wire connections may now be created in the following way. Before creating the connections, enable the two menus **Preferences / Instant net name** and **Preferences /Instant wire label**. Right click and select tool  **Connect component.**

2. Routing the wire connections

a. Enable  **Pin to Pin** whenever an entry or pin is clicked for making a connection. This ensures that the connection is made to the pin.

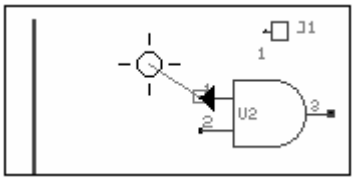


Fig. 4.11

An input box appears prompting the user to enter the name of the net, enter A,n (simply entering A will also suffice). Now select Option tool  **Snap Wire by 90 degree** and click on the workspace where the wire segment has to be bent, now unselect this tool, enable the option tool  **Allow T-connections** and click on the Bus. An input box will ask which member of the bus the wire has to be connected to, enter '0'. A text '0' is tagged to the cursor, place it near the wire.

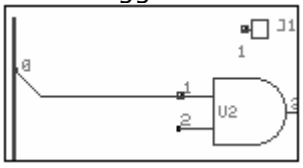


Fig. 4.12

b. Repeat the same process for the second input pin of the AND Gate, in this case give the net name B.
c. Repeat the same process for the first input pin of the XOR Gate. Give the net name A,
d. EDWin gives a message **"Connect to existing Net : A".** Press "**Yes**".
e. Repeat the same process for the second input pin of the XOR Gate and give the net name B.
f. Enable **Pin to Pin** (or press **F3**) and click on the output pin of the AND Gate, enter net name CARRY, now enable **F2**, stretch the wire to a suitable length and left click. Now terminate the connection by pressing END or F4 key on the keyboard or click on the tool **End Connection.**

3. Routing the wire connection without any visible traces

a. Enable the option tool **Connect without wire** from **Connect component** function tool.
b. Click on the pin to start connection. The pin is highlighted and the wire extends with the mouse.

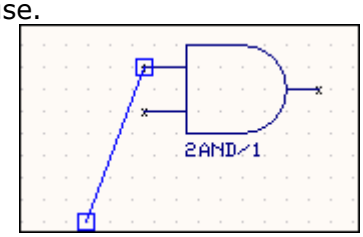


Fig. 4.13

c. Bring the wire end to the required pin and click and then click on **End Connection**. The pins as well as the node get highlighted (Refer Fig. 4.14 & 4.15).

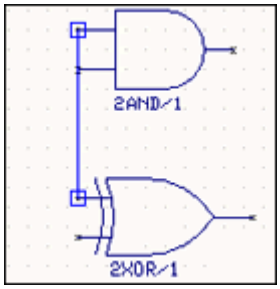


Fig. 4.14

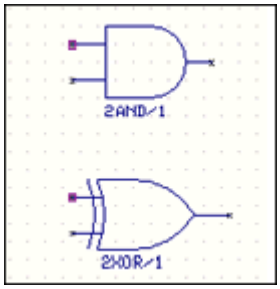


Fig. 4.15

4. Automatic Connection Establishment

Auto routing can take place only if nets exist.

1. Select the option tool Autoconnect wire to connect a single net or Autoconnect all wires to connect selected nets.
2. The Autoconnect dialog box pop up and select the required scheme and click apply.

Tips: To perform any editing operation on the wire drawn, select the wire by using Ctrl key. Bullets get placed on the wire. Bullets have function such as Disconnect wire, Insert Bend point, relocation, etc.

Entering Net labels

To improve the readability of the circuit, use the option tool **Add /Edit net / Bus** member label from the function tool **Edit Connection** and click on the wire to be labeled. The net name is tagged to the cursor. Place the net name at the desired location. Enabling Preferences / Instant wire label achieves this but when it comes to bus connections, it keeps the bus member label instead of the net label. To put the net names in such cases, use this function tool.

Operations that may be performed on a Net

- *Splitting Nets*
  This function tool may be used to split a net into two parts.
  When a net is split then the portion of the net from its starting point to the point of split will retain the same net name whereas the remaining nodes will be assigned to a new net. The new net is automatically assigned a name, which may be changed.
- *Merging Nets*
  Existing nets may be merged using this facility. While merging, priority is given to PWR/GND, named and then to unnamed net.
- *Deleting Nets*
  Allows deleting a node or a whole Net.
- *Net Properties*
  Displays the properties of a selected Net, like Net name, status, bus member etc.

How to merge nets?

i. Select **Edit Connection** function tool of connections and the select the option tool **Merge Net**.
ii. Click on any node of a net (say UN1). This net gets highlighted.
iii. Now, click on any node of the other net (say UN2) which is to be merged to the already selected net (UN1).
iv. A confirmation box pops up. Click yes.

How to split nets?

i. Select Edit Connection function tool of connections and the select the option tool Split Net.
ii. Click on the wire segment that is to be splitted. The whole net appears selected.
iii. Again, click on it. The selected wire segment thickens to indicate that this wire is to be splitted from the rest of the wires of the same net.

iv. A window pops up where the name is edited.

How to delete an existing net?

Select **Delete Whole Net** or **Delete Single Node** from the function tool **Delete Connections/Label** to delete net or a node respectively and click on the nodes. This action deletes the associated wire segment(s) also.

When a net is deleted, the corresponding trace segments also get deleted. The converse is not possible i.e. when a trace is deleted the nodes (net) remains unaffected

How to set net properties?

i. Select Connection Property.
ii. Click on the node/wire. This pop ups the "Property Nets (Layout)" window.

Entering Page and Design Notes

Select the tool **Page Notes** in Tools toolbar to enable a set of tools for creating page notes.

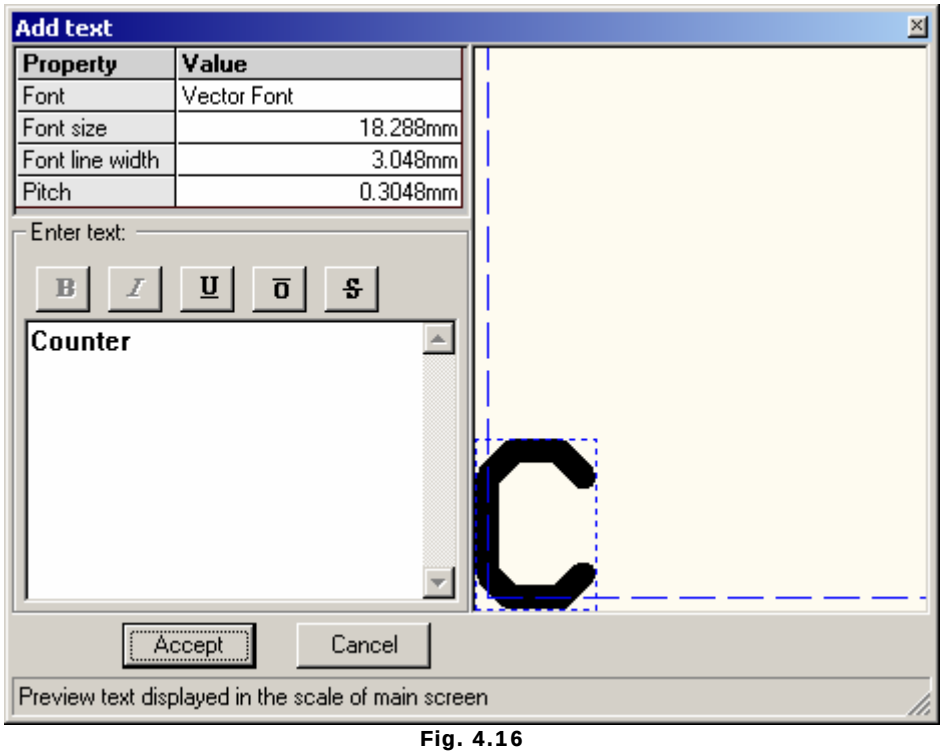


Fig. 4.16

Right click and enable  **Create PN Graphic Item** tool and select the tool  **Create Text** to open a window Add Text as shown in Fig. 4.16. Enter the required notes and accept it.

The text gets tagged to the cursor. Now place the text at desired position. To edit this text, press Ctrl key and click on the text to select it. Perform the various operations using bullets.

Tip: Page notes appear only on the current page (e.g. Page No.) of the project whereas Design notes appear on all the pages (e.g. Project name) of the selected circuit. To enter the design notes, select Design Notes from Tools toolbar. Enter design notes using the same tools explained for page notes.

Property window

The property window like in any other windows program enables the user to change various properties of selected object on the workspace at a single stroke. Selecting the object using Ctrl key and a click enables the user to invoke the property window either on a click after selecting (bulleting) the object or from Edit menu. This section details the purpose and operation of how to invoke the property window of the selected (bulleted) object on the workspace.

Purpose

To edit the properties of object(s) after selecting in the Schematic Diagram. Selecting the object(s) by using Ctrl or Shift key, the object(s) or the block is marked with a bullet. Bullets are small filled rectangles attached to certain strategic points on an object.

☛How to invoke property window and edit properties of Schematic component?

Select (by bulleting-Ctrl+click) the component first and right click on the workspace. In the pop up menu, choose Properties → Schematic Component to display the Property window as shown in Fig.4.17.

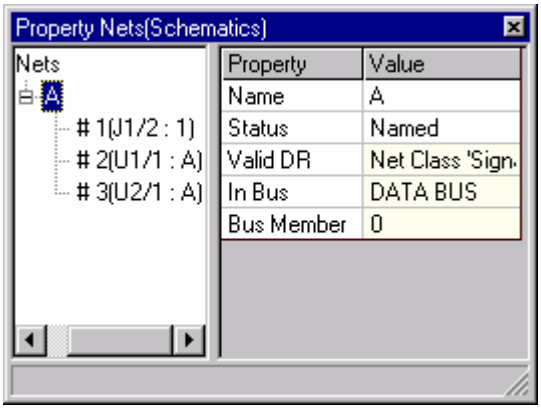


Fig.4.17

The net name and status can be edited.

In the left pane of the property window, right click on the net name pops up a menu as shown in Fig.4.17.

Schematic Component — When more than one component is selected (bulleted), all components get listed on the left side of the Property window under Schematic Components. Selecting each component displays its own properties. But, most common properties like (pack, unpack and repack) may be executed by clicking the right mouse button on Schematic Components (present on the left-hand side of the Property window). Similarly, on the right pane vector position, alignment in the X,Y direction and lock/ unlock of the components may be specified.

Name — Displays the name of the Schematic symbol tagged to a number (\1). Before packing, this number signifies the number of similar components placed like for e.g.:- 2NAND\1,2NAND\2,2NAND\3 etc.. and after packing, it signifies the group it belongs to.

Part — Displays the Part name. We can change the reference of the Part, by entering another Part name in this field. System searches the entire library included in the Search Sequence and displays the part name if available.

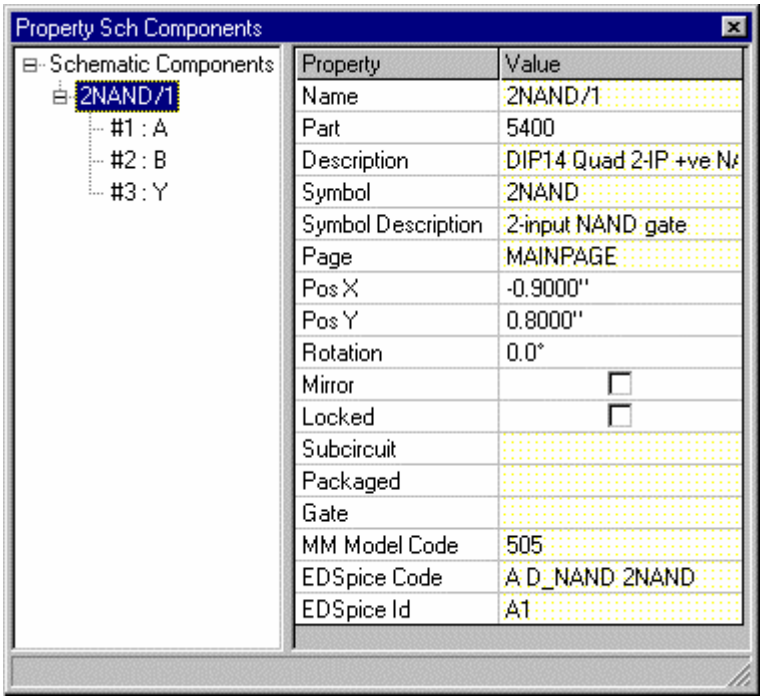


Fig.4.18

Description — Displays the part description that contains the information of the package and symbols used by this part if available. These information's are given at the time of part creation.

Symbol — Displays the name of the symbol.

Symbol description	Displays the symbol description. These information's are given at the time of symbol creation.
Page	Displays the Page in which the selected symbol is placed.
Pos X	Displays the current position (X,Y) of the component with respect to the reference point (by default it is the center of the page). Entering new values may change the position of the component.
Pos Y	Displays the current position (X,Y) of the component with respect to the reference point (by default it is the center of the page). Entering new values may change the position of the component.
Pos Y	Displays the current position (X,Y) of the component with respect to the reference point (by default it is the center of the page). Entering new values may change the position of the component.
Rotation	The component may be rotated by specifying the angle or by selecting the required angle from the list.
Mirror	Checking this option may mirror the component.
Locked	Checking this option may lock the component relocation.
Subcircuit	Displays the subcircuit that is attached to the symbol.
Packaged	This option displays the packaging information of the selected component.
Gate	Displays the gate number the symbol belongs to.
MM Model Code	If the symbol is assigned a modal code in Mixed mode Simulator or EDSpice code or EDSpice ID then these are displayed in the corresponding field.
EDSpice code	If the symbol is assigned a modal code in Mixed mode Simulator or EDSpice code or EDSpice ID then these are displayed in the corresponding field.
EDSpice ID	If the symbol is assigned a modal code in Mixed mode Simulator or EDSpice code or EDSpice ID then these are displayed in the corresponding field.

When more than one component is bulleted, all components get listed on the left side of the Property window under Schematic Components. Selecting each component displays its own properties. But, most common properties like (pack, unpack and repack) may be executed by clicking the right mouse button on Schematic Components (present on the left-hand side of the Property window). Similarly, on the right-hand side, vector position, alignment in the X,Y direction and lock/ unlock of the components may be specified. The information regarding the entry pins of each component may be obtained by clicking on the + icon before each component. This lists all the entries for the each component. Each entry may then be selected to display information such as Pin Number, Pin Attributes, Net Name and the Mixed Mode Sim Name.

☛How to invoke property window and edit properties of Schematic component text?

Bullet the object first and right click on the text. In the pop up menu, choose Properties | Schematic Text to display the Properties window as shown in Fig.4.19.

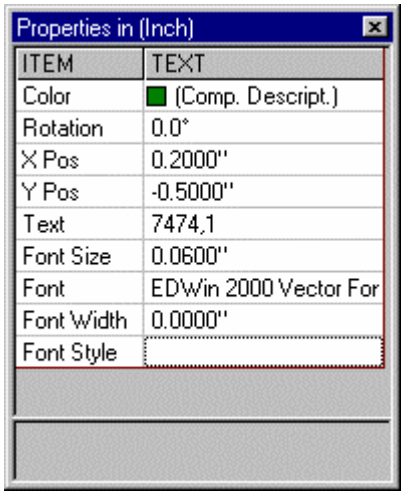


Fig.4.19

Color Displays the color of the selected text. Color may be selected from the Palette.

Rotation The text may be rotated by specifying the angle or by selecting the required angle from the list.

X Pos Displays the current position (X, Y) of the component with respect to the reference point (by default it is the center of the page). Entering new values may change the position of the component.

Y Pos Displays the current position (X, Y) of the component with respect to the reference point (by default it is the center of the page). Entering new values may change the position of the component.

Text Displays the text of the selected item and allows to edit the text.

Font size The size of the text may be selected or specified.

Font The font for the text may be specified.

Font width Allows specifying the font width.

Font style The style whether Bold, Italics, Underline or Strike through may be selected.

Saving the Project

In order to prevent loss of work, save the project periodically using the following steps.

- On the **File** menu of **Project Explorer**, click **Save Project** or Press **Ctrl + S**.
- The first time Save Project is selected, a dialog pops up prompting to enter the name for the project.

- Type in the name of project as **Half_Adder.EPB.**

Printing the Schematic Diagram

To print the Schematic diagram, select **File/ Print page** from the main menu of Schematic Editor. A window pops up with the preview of circuit diagram. Click on **'Fit to single page'** icon. Click on **Print** icon to print the page.

Miscellaneous

Operations that may be performed after placing a component

☛How to change the position of a component?

After placing component on the working area, its position can be altered in one of the following two ways:

- Using Bullets
    i. Press Ctrl and click on the component. The component gets selected indicated by a bullet (blue filled square).
    ii. Move the mouse over the bullet. The shape of the mouse pointer changes from normal pointer to move.
    iii. Click at this point and relocate the component wherever required.
- Using Relocate function.
    i. Select  Relocate component function tool.
    ii. Click on the component to be relocated. The component gets tagged to the cursor.
    iii. Move the mouse and click at the desired location or click on different option tools of Relocate to rotate or mirroring the component.

☛How to Relocate components in block?

Block Relocation may be executed in the following two ways:

- Using Bullets
    i. Press Shift and click the mouse. A square gets tagged to the cursor.
    ii. Drag the square to enclose the required components.
    iii. Click the mouse once again to anchor the block. The block is selected marked with a bullet (blue filled square) at the anchored point.
    iv. Move the mouse over the bullet and observe the shape of the mouse pointer to change from normal pointer to move.
    v. Now relocate the block wherever required

Once when an object(s) is selected or rather bulleted, you are unable to proceed with your work, unless ESC key is pressed.

- Using Relocate function
    i. Select  Block from Tools.
    ii. Select function tool  Relocate Block and click on the workspace.
    iii. Block the components and move to the required position.
    iv. Click the mouse left button to place the block.

How to Repeat a component?

A component already placed on the workspace may be repeated using the tool  **Repeat Component** from **Add Component to circuit** function tool .

i. Select the tool and click on the component. A copy of the component tags to the cursor.
ii. Move to the required location and click to place the component. Another copy remains attached to the cursor unless **ESC** key is pressed.

Step repeat component:

If required, a component may be repeated to the required number by giving necessary details. This is achieved by using the option tool  **Step Repeat Component** of this function tool. The number of components required is entered in the dialog box specifying the number of rows and columns.

How to Delete components?

Deletion may be executed in the following two ways.

- Using Bullets
    i. Press Ctrl and click on the component. The component is selected indicated by a bullet (blue filled square).
    ii. Similarly, keeping the CTRL key pressed select the component one by one.
    iii. When the required components are selected, right click on the workspace to pop up a menu.
    iv. Select Delete function.

This method is preferred if you want to delete components in a series placed all over the workspace where block deletion is infeasible.

- Using Delete function tool
    i. Select the function tool  Delete component tool.
    ii. Click on the component.

In both the above methods a confirmation box pops up to confirm deletion.

How to delete components enclosed in block?

Objects enclosed in block may be deleted by the following two ways.

- Using Bullets
  - i. Press Shift and click the left mouse button. A square gets tagged to the cursor.
  - ii. Drag the square to enclose the required components.
  - iii. Click the mouse once again to anchor the block. The block gets selected indicated by a bullet (blue filled square) at the anchored point.
  - iv. Right click on the workspace and select Delete function.

Once when an object(s) is selected or rather bulleted, you are unable to select tools and menus, unless ESC key is pressed.

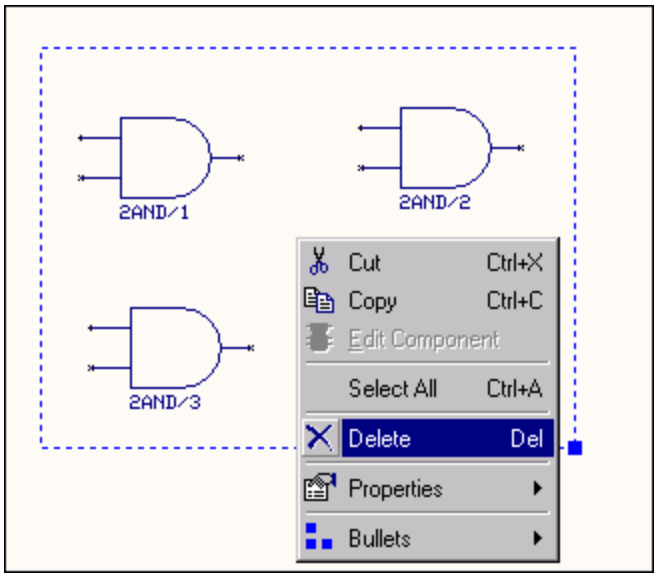


Fig.4.20

- Using Block Delete function tool.
  - i. Select Block from Tools.
  - ii. Select the function tool Block Delete.
  - iii. Enable the option Delete Components in Block and click on the workspace.
  - iv. Block the components and release the mouse button.
  - v. In both the above methods, a confirmation box pops up to confirm the delete operation.

Select the appropriate option tool(s) to delete the desired object(s).

How to Lock/Unlock components?

Tampering of components placed in the working area can be avoided using **Lock/Unlock Component** function tool. Lock/Unlock by prefix allows locking/unlocking of all the components having the same prefix.

Lock component

i. Select the option tool **Lock by prefix**. A window pops up where the name prefix by which components are to be locked is entered.
ii. Type the prefix name and click ***ACCEPT*** to lock the components.

Unlock component

i. Select the option tool **Unlock by prefix**. A window pops up where the name prefix by which components are to be unlocked is entered.

Type the prefix name and click **ACCEPT** to unlock the components.

How to change the reference?

The reference of the components loaded can be changed using any one of the following methods.

- Using Library Browser/ Explorer.
  i. Open Library Explorer or Browser and click on the component present in the search list.
  ii. Press Alt key and drag the component from the Browser or Explorer to the editor and move anywhere over the component which is required to be replaced.
  iii. Now, release the mouse.

- Using Bullets
  i. Bullet a component (presses Ctrl and click on the component). Right click anywhere on the workspace.
  ii. A menu pops up from which select Properties/ Layout Component. Property window pops up where various options are provided for the bulleted component(s) and its entries.
  iii. To change the reference, type the required Part name in the Part field. Press enter or click the next row.
  iv. The part on the schematic editor is replaced if the component name typed is available in the System Library.

☛How to find a component?

Following are the two methods to find a component.

- Select Component from Redraw drop-down available in Standard toolbarStandard_Tool_Bar to pop up a window. Type in the Component name and the group number separated by /. For E.g.: U1/1
- This method is much advanced and is obtained by pressing Ctrl+F on the workspace. A window is displayed wherein the information regarding all components are displayed.

Operations that may be performed on a trace after routing

Relocate segment – Use the tool  **Relocate segment/ Bend point** to relocate the connection segment / bend point after routing.

Reroute trace - Use the tool to  **Reroute Connection/bus to reroute** the existing route path.

Special Operations

☛How to select connection(s)/ nets(s) by marking with bullets

Press Ctrl and click on the connection. Now each connection segment of the same net appears bulleted. Each segment is marked with three bullets.

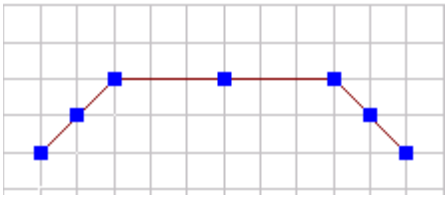


Fig.4.21

Each bullet placed on either ends of the connection segment performs move operation whereas the bullet at the center allows inserting a bend point.

Following are the special operations that may be performed when a connection is bulleted.

1. Move the mouse over the bullet. The normal mouse pointer will now change into move/ insert mouse pointer. Click the mouse on this bullet and relocate/ insert the connection and place by releasing the mouse.
2. When an object(connection) is bulleted, its properties may be accessed in the following way:

Right click on the bulleted trace. A menu pops up.

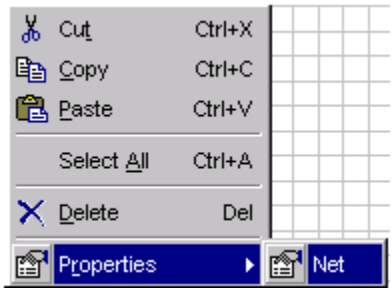


Fig.4.22

Menus such as cut, copy, paste, delete, select all does the function as the name signifies and is similar to any windows program. The property menu lists a single instant of all objects bulleted on the workspace. To obtain the properties of trace/ net, click **Property→Net.**

Once when an object(s) is bulleted, you will be unable to work with tools and menus, unless the bullets are removed.

To remove bullets placed on the object press ESC key or keeping the CTRL key pressed, click on the bulleted object again.

Properties of a connection

How to invoke property window and edit properties of trace?

Select (bullet) the object (trace) first and right click on the trace. In the pop up menu, choose **Properties/Trace** to display the property window as shown in Fig.4.23.

Name	Display the name of the net. This may be changed.
Status	Display the status of the net whether named unnamed or Pwd/Gnd.
In Bus	Displays the bus name to which the selected connection (net) is connected.
Bus Member	Displays the Bus Member Number with which the selected net is identified.

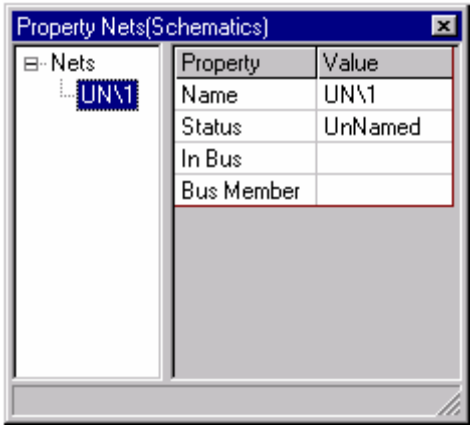


Fig.4.23

Property window is also invoked when you double click on the object (components, traces, text copper pour item etc.) provided the selected tool on the toolbar does not perform any function.

How to select text/Design/ Page Notes(s) by marking with bullets?

Press Ctrl and click on the texts/ notes. Now the texts/ notes appears selected with three bullets marked one on each end and at the center as shown in fig.4.24.

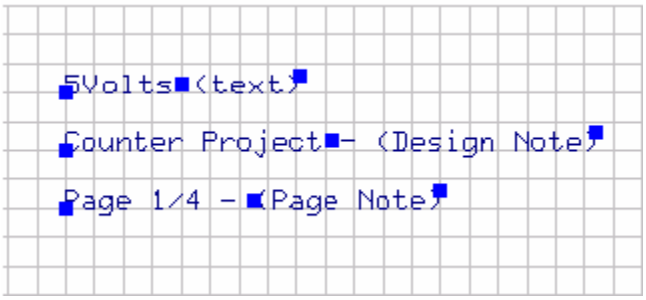


Fig.4.24

E.g. of Text, Design and Page notes
Similarly, keeping CTRL key pressed, click on other text/ notes. All clicked text/ notes appear selected with three bullets marked on each text/ notes.
Following are the special operation that may be performed when an object is bulleted.

1. Move the mouse over the bullet present on the left end of the object. The normal mouse pointer changes to MOVE mouse pointer. Click the mouse on this bullet and relocate the text/notes to the required position. Place the text/notes by clicking the left mouse on the workspace. Similarly move the mouse over the bullet at/ on the center/ right end. The mouse pointer will change to CHANGE/ STRETCH mouse pointer. Click to pop up

2. When an object is bulleted, its properties may be accessed in the following way: Right click on the component. A menu pops up as shown in Fig 4.25.

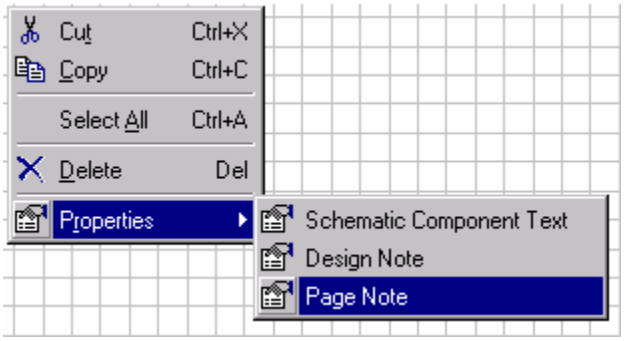


Fig.4.25

☛How to select Page format by marking with bullets?

Press Ctrl and click on the page format. Now the page format appears selected with three bullets marked one on each end and at the center of side.
Following is the special operation that may be performed when an object is bulleted.

Move the mouse over the bullet present on the left end or right end of the page. The normal mouse pointer changes to MOVE mouse pointer. Click the mouse on this bullet and relocate the page outline segment to the required position. Place the segment by clicking the mouse on the workspace. Similarly move the mouse over

the bullet at the center. The mouse pointer will change to INSERT mouse pointer. Insert as many as bend points required and click to end adding bend points.

Once when an object(s) is bulleted, you will be unable to use tools and menus, unless the bullets are removed.

To remove bullets placed on the object press ESC key or keeping the CTRL key pressed, click on the bulleted object again.

How to select Bitmap by marking with bullets?

Press Ctrl and click on the bitmap. Now the bitmap appear selected with a single bullet marked on one side of the bitmap. Move the mouse over the bullet. The mouse pointer changes to MOVE pointer enabling the user to relocate to the desired position. Click the mouse to place the bitmap at the required position.

Once when an object(s) is bulleted, you will be unable to use tools and menus, unless the bullets are removed.

How to Save and Load a block?

To save block

i. Select  Block from tools.
ii. Select  Save Block function tool
iii. Block the components required to copy

EDWinXP Save Block File window pops up, give a name for the block file to be saved, for example GATES.ESB and click save.

To load block

i. Select  Block from tools.
ii. Select  Load Block function tool
iii. Select stored block file from EDWinXP Select Block File to Load window that pops up.

Chapter – 5

Introduction to Simulation

The Purpose

Simulation provides a detailed analysis of the circuit behavior. For the virtual simulation of a circuit, the real model of the circuit is created by taking all factors into consideration, and the appropriate inputs are given. Then the outputs at each level are checked and corrections or modifications are made.

EDWinXP provides two types of Simulators. **The Mixed Mode Simulator** may be used for simulating analog and digital circuits. The **EDSpice Simulator** is provided for the users who prefer to work with SPICE.

SPICE is an acronym for **Simulation Program with Integrated Circuit Emphasis**, developed by University of California, Berkeley. SPICE is an important tool for learning circuit analysis and design, and for testing electronics circuits.

EDSpice Simulator provides the facility to analyze and validate behavior of circuits captured in the form of Schematic diagrams using SPICE.

It is possible to view the analysis in the virtual *Cathode Ray Oscillograph* available with the simulator. This multi channel Oscillograph gives a running waveform and it is possible to change the element parameters and view the changes while running the simulation.

Waveform Viewer is used to display and postprocess the results of analyses in graphical form and if required, the results may also be presented textually.

Types of analysis supported by EDWinXP

The different types of analyses that can be done in EDWinXP are listed below. The simulator that supports the analysis is given in brackets i.e. Name of analysis (Simulator name-MMS or EDS). MMS-Mixed Mode Simulator, EDS is EDSpice Simulator.

Bias Point Calculation (MMS)/ Operating point Analysis (EDS)

A **Bias Point Analysis / Operating Point Analysis** is the simplest analysis that can be done using the Simulator. It is used to determine the DC behavior of a circuit; in other words, the DC bias conditions.
When the analysis is performed, all capacitors are open-circuited and inductors are short-circuited for calculating the values. This is because a bias point analysis is performed using DC values, at which inductors are effectively short circuits, and capacitors are open circuits. The values generated remains until next preprocess is

given. This is the reason why; it is necessary to preprocess once the circuit topology is changed.

 *Even though the bias point calculation is not done this is analysis is automatically done during AC and Transient analysis.*

Transient Analysis (MMS and EDS)

The transient analysis computes the transient output variables (voltage and current) as a function of time over a user-specified time interval. The initial conditions are automatically determined by a dc analysis. All sources which are not time dependent (for example, power supplies) are set to their dc value. The transient time interval is specified on a control line.

Transfer Function Analysis (MMS)

The transfer function analysis calculates the small signal ratio of the output node to the input source. This is done along with Transient analysis.

Transfer Function Analysis (EDS)

The transfer function analysis calculates the small signal ratio of the output node to the input source, and also the input and output impedance of a circuit. This analysis may be used to determine the small signal gain and the input and output impedance of filter circuits. Any nonlinear models, such as diodes or transistors, are first linearized based on the DC bias point, and then the small signal DC analysis is performed.

Parameter Analysis (MMS)

This analysis calculates the change in the output of a given circuit when a selected parameter of a particular circuit element is varied over a range of values. The corresponding output is plotted just as in the case of Transient analysis. The variation in the parameter value can be done in two ways:

1. Sweep, where the start and end values of the parameter can be entered and analysis is carried out in the specified step value.
2. Step, where the different parameter values for which analysis is to be performed can be specified.

Fourier Analysis (MMS/EDS)

This performs a Fourier analysis of an output variable when done with Transient analysis. Computes the amplitudes and phases of the first nine frequency components (harmonics) of a user-specified fundamental frequency, as well as the DC component.

DC Sweep Analysis (MMS)

This is a non-linear analysis, which determines the DC operating point of the circuit. Capacitors are open-circuited and inductors are short-circuited during DC analysis. One or more sources (current and voltage) may be stepped over a range. Results of the analysis at each source value may then be viewed in the waveform generator.

It is used for obtaining the small signal DC bias solution of a circuit, as one independent source sweeps over a range of values. It is also often used for obtaining the characteristic output curves of semiconductor devices.

AC Sweep (MMS)/Small Signal AC Analysis

AC Sweep analysis is a linear small-signal analysis, over a user defined frequency range, and based on the linearized small signal AC model values of all circuit elements at the operating point. It is used to obtain the small signal AC behavior of the circuit. This can be used to study the frequency response, gains, Trans impedances, Bode Plots, etc. of a circuit. It can also be used to know the phase changes in a circuit. The various output modes are magnitude; phase, real, imaginary and 20log of gain.

Monte Carlo (MMS)

The Monte Carlo analysis is used for simulations with a given error on different components. This test is very useful for visualizing how the circuit will run if imperfect components as are used in reality. The Monte Carlo analysis allows the user to input two things:

- The percent error of a given circuit element can be defined. This is the purpose of the Monte Carlo Analysis, i.e. to apply an error to components. If the finished product will have resistors with a 5% error, the simulation can include this deviation.
- The type of error can be defined as either Gaussian (normal), or Uniform. The Gaussian mode of simulation is more realistic than the uniform mode. The Gaussian mode uses a bell curve approach as it randomly pick values in the range of error specified but with the majority of the values near the resistor value.

  The Uniform mode of deviation randomly selects values within the range specified oblivious of what the actual value of the resistor is. This mode of deviation is more suited for a situation where the value of the resistor is not known precisely.

Sensitivity Analysis (MMS)/ DC/AC Sensitivity Analysis (EDS)

This will calculate sensitivity of an output variable (voltage and current) with respect to all circuit variables, including model parameters. This calculates the difference in an output by changing each parameter of each circuit element independently. This also displays the highest sensitive element in the circuit.

DC Transfer Function Analysis

A DC Transfer Function Analysis is used to obtain the variation in circuit voltages and/or currents, with respect to variations in either one or two, independent source/s, at DC Bias conditions. It is used for obtaining the small signal DC bias solution of a circuit, as one (or two) independent source sweep over a range of values. It is also often used for obtaining the characteristic output curves of semiconductor devices.

Noise Analysis (EDS)

The noise analysis does analysis of device-generated noise for the given circuit. When provided with an input source and an output port, the analysis calculates the noise contributions of each element (and each noise generator within the element) to the output port voltage. It also calculates the input noise to the circuit, equivalent to the output noise referred to the specified input source.

Distortion Analysis (EDS)

The distortion analysis computes steady-state harmonic and intermodulation products for small input signal magnitudes. If signals of a single frequency are specified as the input to the circuit, the complex values of the second and third harmonics are determined at every point in the circuit. If there are signals of two frequencies input to the circuit, the analysis finds out the complex values of the circuit variables at the sum and difference of the input frequencies, and at the difference of the smaller frequency from the second harmonic of the larger frequency.

Pole-zero Analysis (EDS)

A Pole-Zero analysis is used to compute poles and zeroes of a small signal AC transfer function of the form $H(z) = \frac{Y(z)}{X(z)}$ of the circuit. Pole-zero analysis is most commonly used for determining the stability of control circuits.

This computes the poles and/or zeros in the small-signal ac transfer function. The program first computes the dc operating point and then determines the linearized, small-signal models for all the nonlinear elements in the circuit. This circuit is then used to find the poles and zeros.

Two types of transfer functions are allowed: (output voltage)/ (input voltage) and (output voltage)/ (input current). These two types of transfer functions cover all the cases and one can find the poles/zeros of functions like input/output impedance and voltage gain. The input and output ports are specified as two pairs of nodes.

General requirements to simulate the circuit

Simulation

Before simulation all the circuit elements used in the project should be identified by the simulator. In SPICE, the circuit elements are identified by the name assigned to each element which in turn will invoke the necessary function (simulation function) associated with the element (This is already made available to the user in SPICE.)

E.g.: In SPICE, a resistor is identified with the program by the Letter R.

Therefore, generally for simulation, a circuit should consist of circuit elements which contain the required simulation information attached and supported by the Simulator. (In Mixed Mode simulator, the simulation information is stored in a 'Primitive' while in EDSpice it is stored in a 'Model'. Both exist in the EDWinXP library in the form of.dll format). Mixed-Mode Simulator marks all components which do not have their primitives as the "non-simulatable components" (marked in red) and ignores them during simulation.

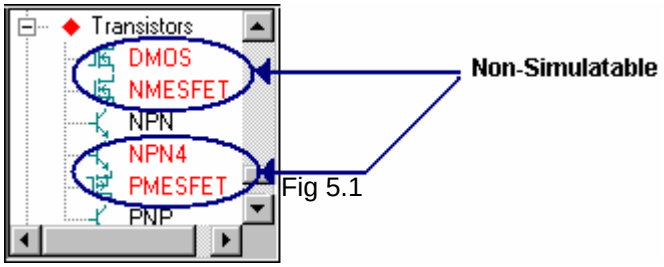


Fig 5.1

Model

This dictates the behavior of a circuit element during simulation. This is available from the model library and the simulation function links the element to its specified model.

Simulation function

It is an integer number identifying a primitive that models this component. A Simulation Function is a sort of identifying tag which tells the simulator that information required to simulate the behavior of a component (Simulation primitive) is available in Library. When a Schematic is created, the Simulation Functions assigned to each of the parts are also loaded.

Simulation Primitives:

The Simulation Primitive contains information required by the simulator to simulate a component. We can simulate only those parts that have a simulation primitive available for it. They are present in the Library Directory in the form of Dynamic Link Library files (*.DLL). The symbol of each component stores the Simulation Function and so does the primitive. At the time of simulation, Mixed Mode simulator searches for a primitive in the library containing this Simulation function and retrieves the required information to simulate the component.

Before simulation, invoke the Preprocess command to make any changes (adding/removing circuit elements) effective.

There are two kinds of primitives: Logic and analog. Logic primitives (gates, flip-flops, counters, etc.) have positive simulation functions. Analog primitives (resistors, inductors, transistors, etc.,) have negative ones. Simulation function equaling to zero is used for non-simulated components.

In addition, all used entries of the symbol must have proper simulation names that match pin names defined in the corresponding DLL simulation primitive module.

Tips: To speed up the simulation it is recommended to simulate separate parts of the project using a number of equivalent electrical schematics.

Preparing the Circuit for Simulation

Several steps are involved when preparing a circuit for simulation. Preprocess the circuit for any change in the schematic to be reflected during simulation.

Placing Test points

EDWinXP allows to place test points and waveform markers in the circuit with the tools available in **Instruments** in either of the editors. (Mixed Mode and EDSpice).

The list of options enables the user to set ground, place test points, add/change value of each element, place markers to display the resultant waveforms after the completion of each analyses, to reassign simulation parameters and so on.

In **Mixed Mode Simulator**, Select **Instruments** | **Test points** to view values of voltage, current, Logic States at specific points, select the option **Set Waveform Contents** to place markers at points where the waveforms are to be displayed. Different options are available to place waveform markers at specific points namely Current, Voltage and Logic Waveform.

For **EDSpice Simulator**, Select **Instruments** | **Probe Results** option to obtain the current/voltage values at specific points in the circuit and **Set Waveform Contents** to place Waveform Markers for current, voltage or logic waveform at places where the results are to be displayed graphically.(Refer the figure given below)

The function tool bar under Instruments and their functionality for Mixed Mode and EDSpice Simulators are given in Fig. 5.2.

Mixed Mode Simulator

Fig 5.2

EDSpice Simulator

Figure 5-3 shows different test point and markers assigned in a circuit in Mixed Mode Simulator.

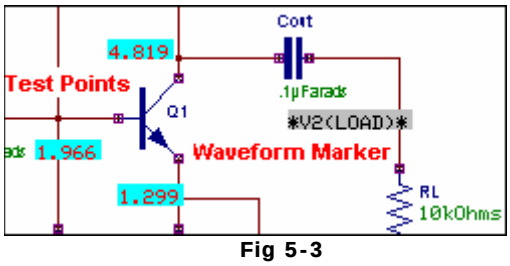


Fig 5-3

Figure 5-4 shows different test point and markers assigned in a circuit in EDSpice Simulator

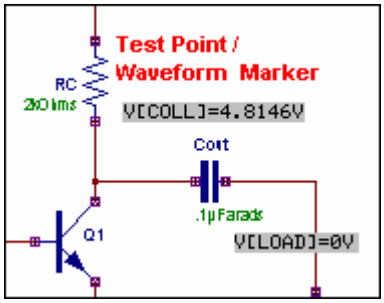


Fig 5-4

Assigning Simulation Parameters

Before initiating simulation on the circuit, the simulation parameters for various circuit elements have to be specified. This is done by selecting the **Component Properties**  Function tool and the option tool **Change Simulation Parameters**  from the list.

With this option enabled click on any circuit element whose parameters have to be changed or assigned and a window pops up (Fig. 5.5) where necessary entries can be made or edited.

In **Mixed Mode Simulator** module, a window as shown in Fig.5.5 pops up. Here, the parameters can be edited, loaded from the library or saved in the system library.

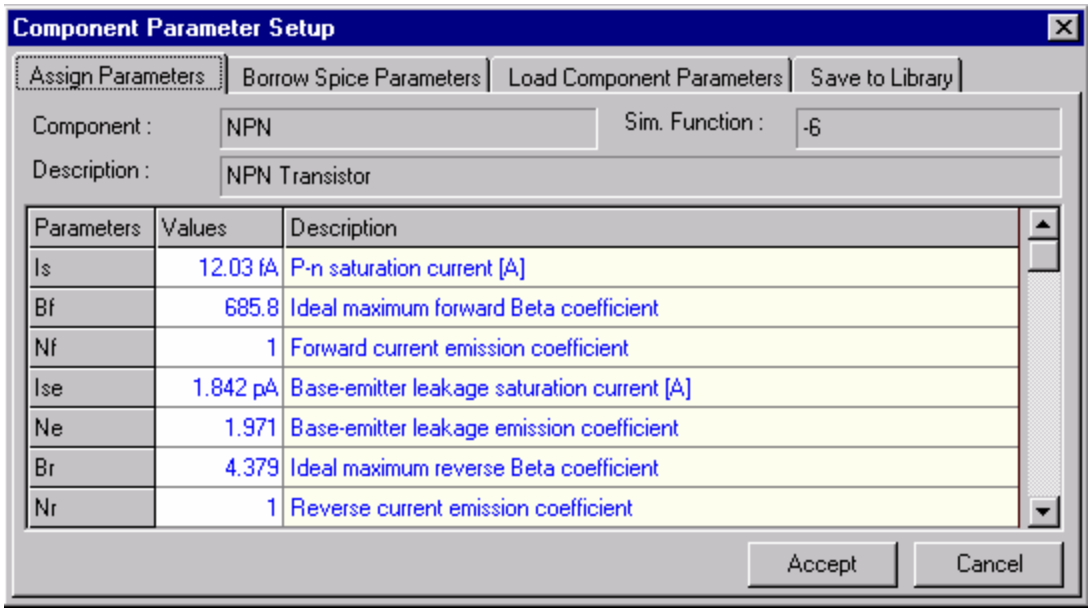


Fig. 5-5

EDSpice Simulator provides options to load models from the system library and also to change the parameters of circuit elements. Enable **Assign Simulation Parameters** option from the **Component Properties** function tool and click on the element and a window pops up where the required changes can be made (Fig. 5-6).

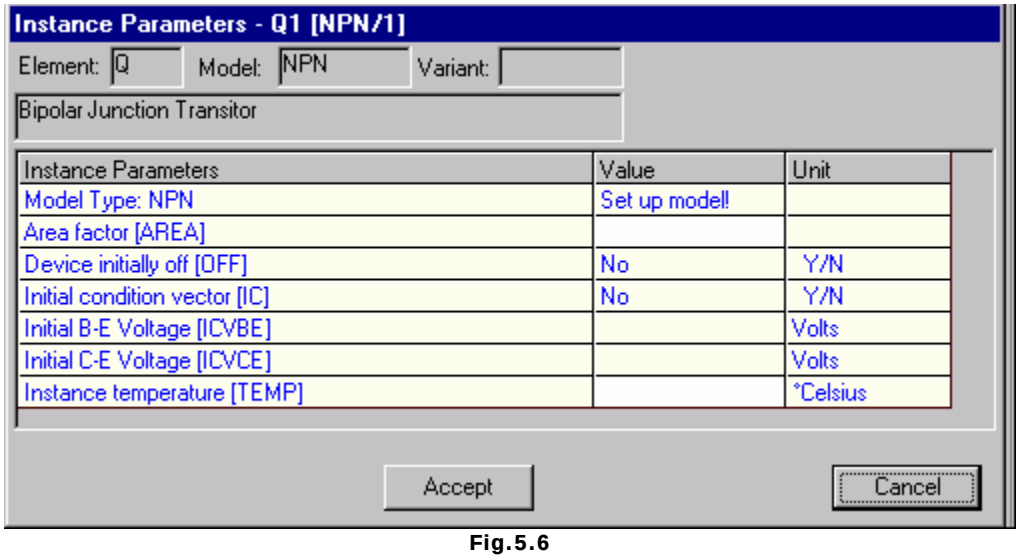


Fig.5.6

When clicked on Set up model you get a window as shown in Fig. 5.7, where when clicked on ***ACCEPT*** the default model is taken or to load spice models from the

system Library, click on **Load** From Library option and load the required model from the displayed list.

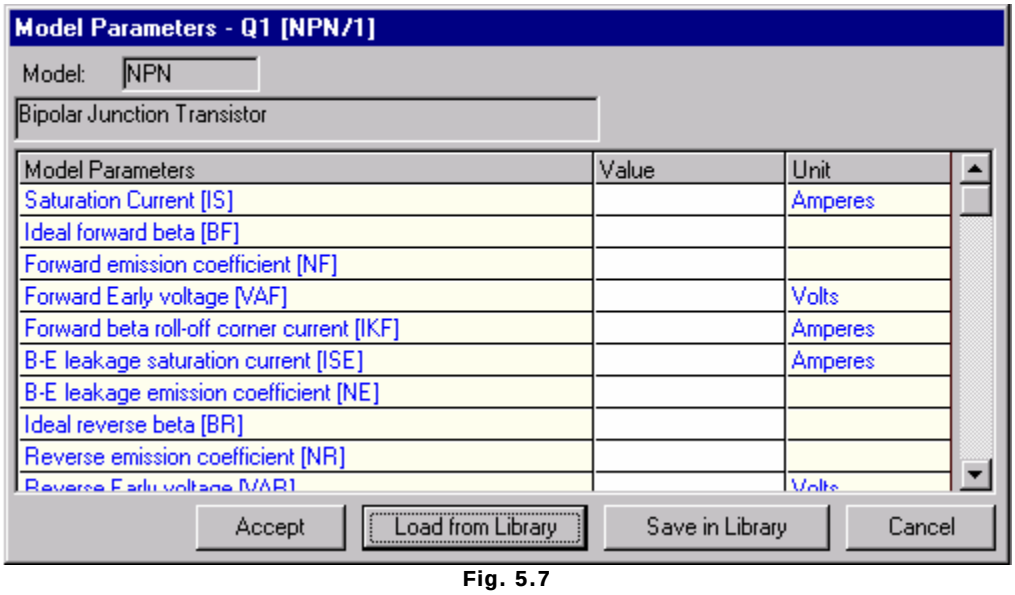


Fig. 5.7

Setting the Input Pulse/Clock

Next, set the input stimuli to the circuit. This can be done by selecting the Function tool **Preset Logic State** and then the Option tool **Clock Generator**. Click on the wire where the input has to be applied.

E.g.: In the case of a Half Adder circuit, it has to be the input wires A and B. Click on A, an input box appears with a drop down list from where the required string for the clock pulse can be selected or a new string can be typed in. Enter the string (L20u, H20u), a label G! gets tagged to the cursor, place it next to the wire A. Similarly click on B and enter the string (L10u, H10u) or select a string from the existing list. (Refer Fig.5-8).

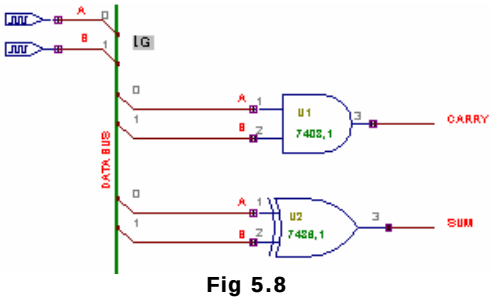


Fig 5.8

Apart from selecting a pulse from the given list one may also set a pulse or clock according to the requirement using the different options provided in the clock editor (Refer Fig. 5-9). Two different set of options are available for setting up a

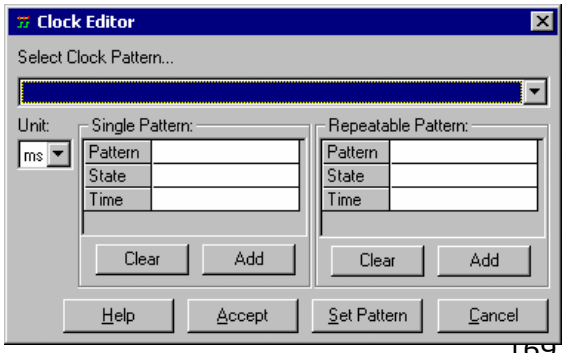


Fig 5.9

pattern either a **single pattern** or a repeated one. A pattern can be set by selecting from the dropdown list L/H/Z (i.e. Low, High, High Impedance). Similarly the duration can be chosen for the pulse in ms/us/ns. Click Add to obtain the pattern and click **Set Pattern** to apply it. Clicking ***ACCEPT*** will affirm the operation.

E.g.: To set a pulse of Low state for 10 ms and High state for 20µs, select the appropriate options and click set. The string appears as: **L10ms, H20us.**

To set a clock, check on the item clock of Low State for 20µs and High for 20µs and click Set. The string appears as :**{ L20u, H20u}.**

This string (**L20u, H20u**) is a clock generator. Since this string is enclosed within brackets, this will repeat the pattern given in the string till the Final Time specified in Simulation menu | Analysis.

The truth table of the Half Adder is as follows

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

In order to test for all the given conditions at one time, the input stimulus can be given according to the conditions specified in the truth table. Let us assign an arbitrary period of say **10µs** for each **Condition** specified in the Truth Table, therefore, within **40µs** (4 conditions x 10µs) the results required for analysis of this circuit is obtained.

A – the column for A is 0 0 1 1, i.e. A should be low for 2 periods and then high for 2 periods. This can be set as **(L20u, H20u)**.

B – the column for B is 0 1 0 1, i.e. B should be low for 1 period and then high for 1 period this can be set as **(L10u, H10u)**.

After the analysis is carried out, the results are either displayed in the **Waveform Viewer**. Right click and select the function tool  **Set Waveform Contents** and then the option tool  **Logic Waveforms**. Now click on net A and place the waveform marker near the wire. Similarly click on the other nets, B, CARRY and SUM and place their respective waveform markers.

Obtaining the results

The results after each analysis can be obtained in the desired format.

In Mixed mode, the results can be viewed in a multi channel Oscillograph in real time or can be viewed in a waveform viewer. Outputs in text format can be viewed in an ASCII file viewer.

In EDSpice Simulator, the results may be viewed either in the waveform viewer or the Logic Analyzer, which allows to get the result in textual format.

Waveform Viewer is used to generate results graphically for **Mixed Mode Simulator** and **EDSpice Simulator**. The Waveform represents the data generated by simulators to present the simulation results in a graphical format. This can be displayed on the screen, print or saved as a part to be placed on the actual schematic drawing.

The functionality of Waveform Viewer (Fig. 5.10) has been enhanced to examine the resultant waveforms of different analyses in a better way. In the Waveform Viewer, there is no limit to the number of variables that can be loaded. At the same time it is capable of handling any number of samples and hence the simulation time has no limit. The Waveforms may be saved to or loaded from a project. Several Waveforms can be tiled together to view on a single screen. Tools have been made available to allow users to change the presentation style of the Waveform with ease.

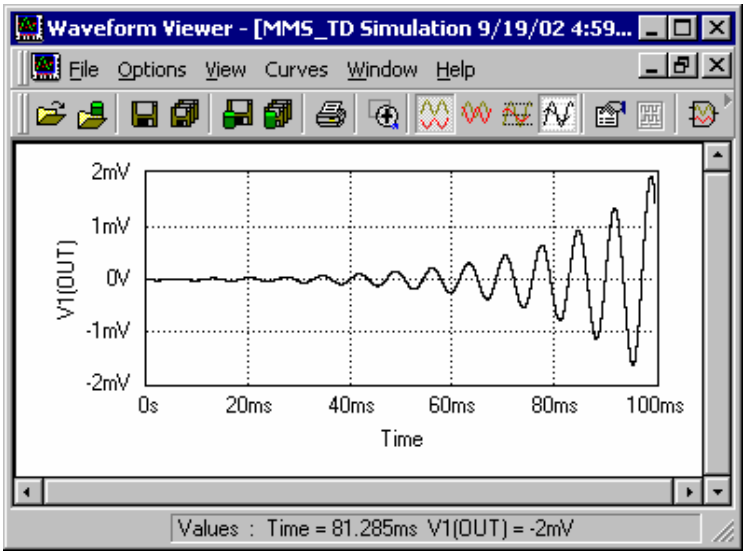


Fig 5.10

Chapter 6

Mixed Mode Simulator

Mixed Mode Simulator, the system's native circuit level analyzer test the functioning of the circuit .This Simulator supports TD, DC, AC Parameter sweep, Fourier, Monte Carlo and Sensitivity analyses of analog, digital, and mixed-signal circuits.

Steps for Mixed Mode Simulation

Create/Load the Project

You can create a new project by using EDWinXP –Main Menu File/New Project. Please Refer Chapter 4 to know more about project creation.
Or Load the existing project using EDWinXP –Main Menu File/Open Project.

Invoking the Mixed Mode Simulator

Mixed Mode Simulator can be invoked from Schematic Editor /Preferences/ Mixed Mode Simulator.

Preprocess the circuit

You can evoke preprocessing from Simulation Menu.

The simulator analyzes the schematic first and checks for the simulation function. It generates the data along with the statistics of the circuit. Data includes the number of digital and analog nets, list of symbols, which may be simulated along with their simulation functions, number of digital inputs and outputs, number of A/D input/ outputs. This is presented as a dialog box. Observe that the analog primitives are assigned negative simulation function.

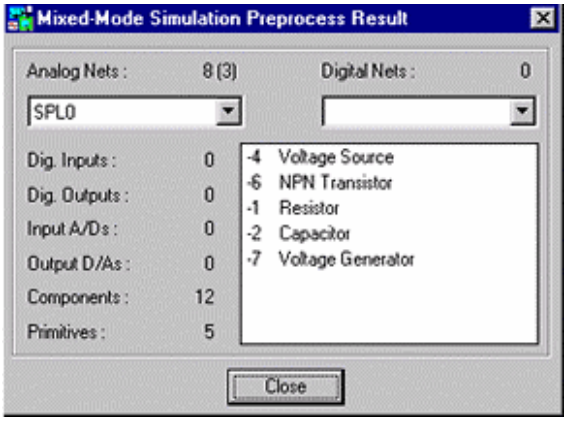


Fig. 6.1

Click the ***Close*** button to close this dialog box. The simulator is now ready for making further analysis on the circuit. (Refer Fig.6.1)

Any change in the circuit element values or topology gets implemented only if the preprocess is invoked. Preprocessing the circuit resets the values set.

Set element value

Before executing the analysis, set the circuit element values. Select the option tool **Change Simulation Parameters** from the function tool **Component Properties** in **Components** or **Instruments** Toolbar and click on the component.

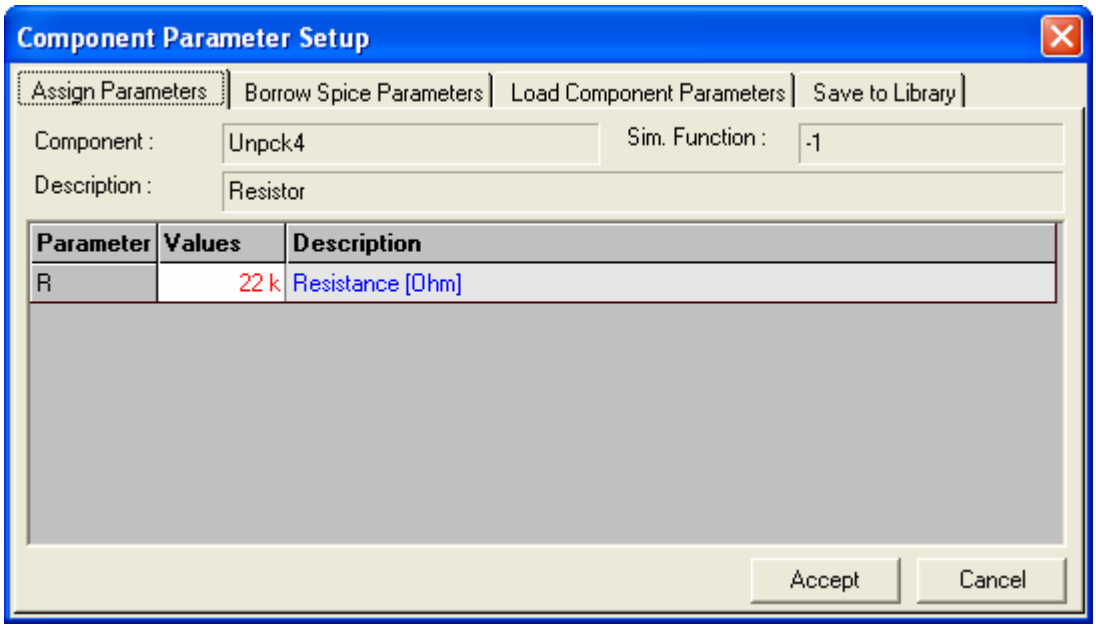


Fig 6.2: Component Parameter setup window

For e.g.: Component Parameter setup window for a resistor is as shown in the figure Now edit the default value by clicking the particular cell. In this way the parameters for each element needs to be assigned.

Place test points/ waveform markers

The analysis result may be viewed at all element nodes by placing appropriate **Test points/** **Set Waveform Contents** (if graphical output is required). After selecting the suitable test points, click on the connection/ pin to assign the test point. Move the small outline rectangle to the desired position to place the test points (Refer Fig.6.3).

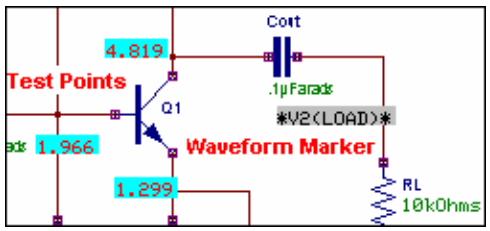


Fig 6.3

Set simulation limits

The default simulation parameters like temperature, iteration limits, and minimum displayable units may be reset using Setup Simulation Parameters. This window can be invoked from **Analysis/General Settings**.

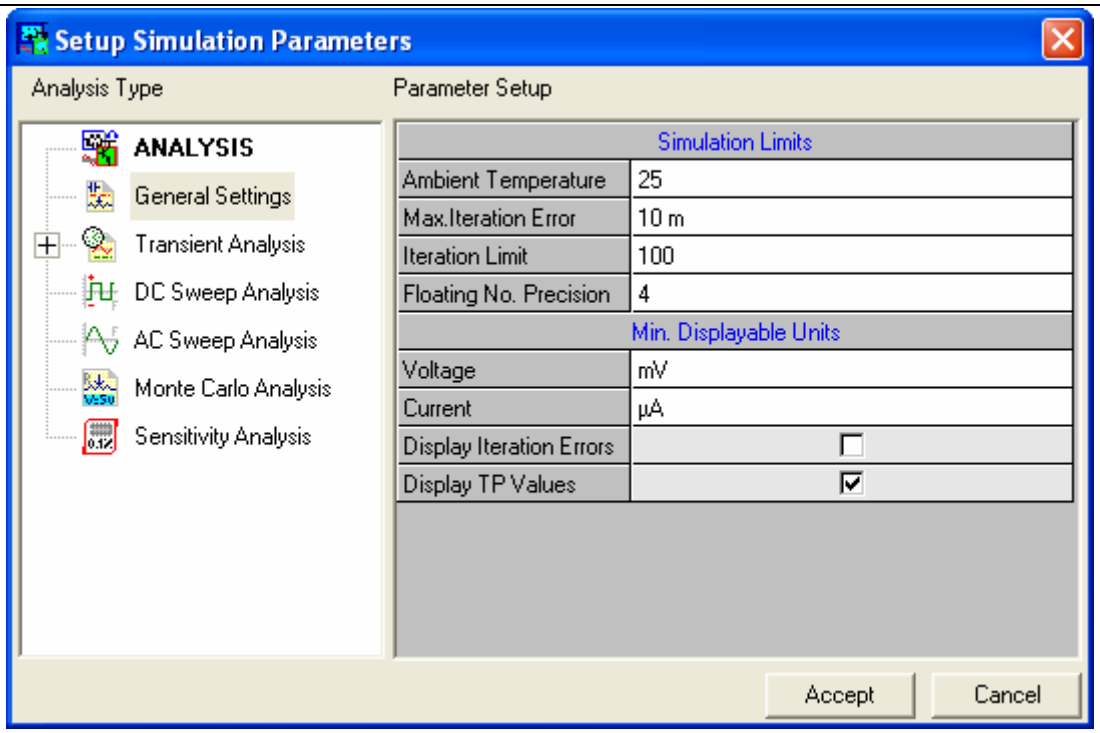


Fig 6.4: General settings

Execute analysis

Invoke Analysis from the **Simulation** Menu and choose the required analysis. Set the parameters and click on ***Accept*** button to execute the Analysis.

Tips: Check Display waveform option to view the result immediately.

Types of Analysis Supported by Mixed Mode Simulator

Mixed Mode Simulator can simulate analog, digital as well as a combination of analog-digital circuits. It is de facto that an analog simulator equipped with a logic simulation engine models the digital parts of a circuit during the Time Domain (TD) Transient Analysis. The commonly used analyses by this simulator are: (Refer Fig.6.5)

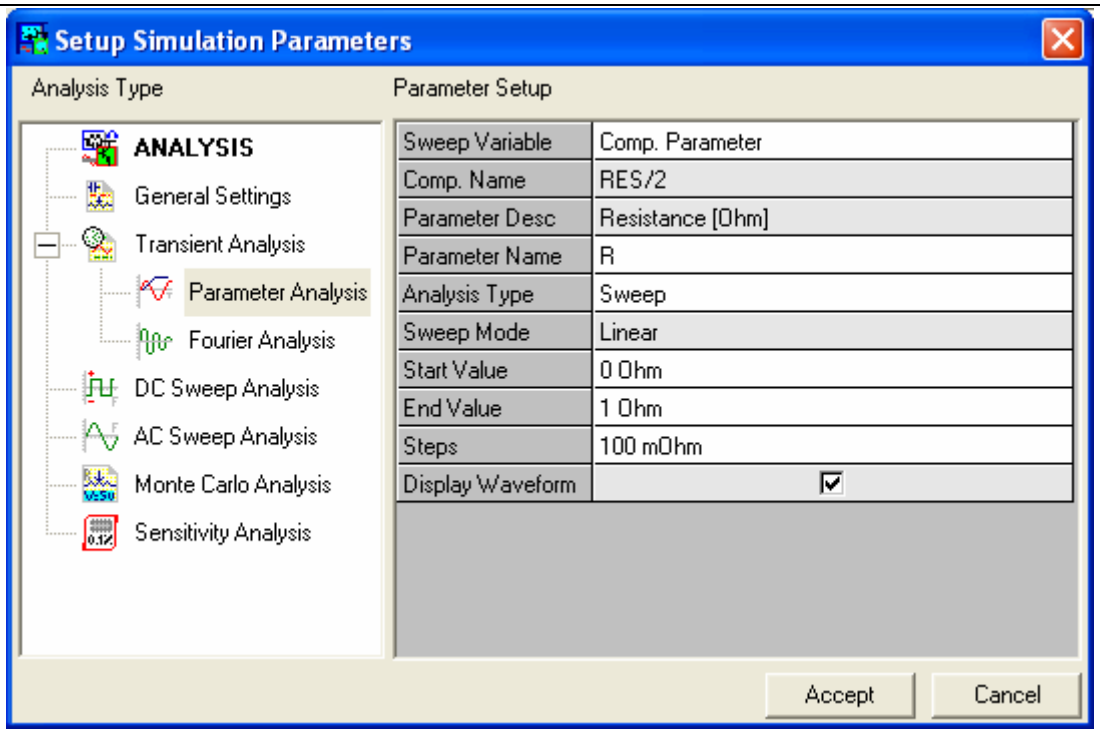


Fig 6.5

- ❑ Bias Point Calculation
- ❑ Transient Analysis
- ❑ Parameter Analysis
- ❑ Fourier Analysis
- ❑ DC Sweep Analysis
- ❑ AC Sweep Analysis
- ❑ Monte Carlo Analysis
- ❑ Sensitivity Analysis

Bias Point Calculation

Please refer sample project (EDWinXP/Job/ MIXMODE_EDSPICE) Amplif.EPB

Steps:

1. Right click and select the  **Test Points** function tool. Select the  **Voltage TP** and place the test points at the base, collector and emitter of the transistor 2N3227 (Refer Fig. 6.6).

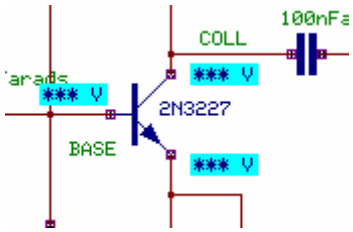


Fig. 6.6

2. To review the 2N3227 transistor parameters, select the function tool  Component Properties and then the option tool  Change Simulation Parameter. Click on the transistor to view the component Parameter Setup of the transistor. These parameters can be modified. Click ***CANCEL*** to exit the dialog box without effecting change and ***ACCEPT*** button for the changes to come into effect.

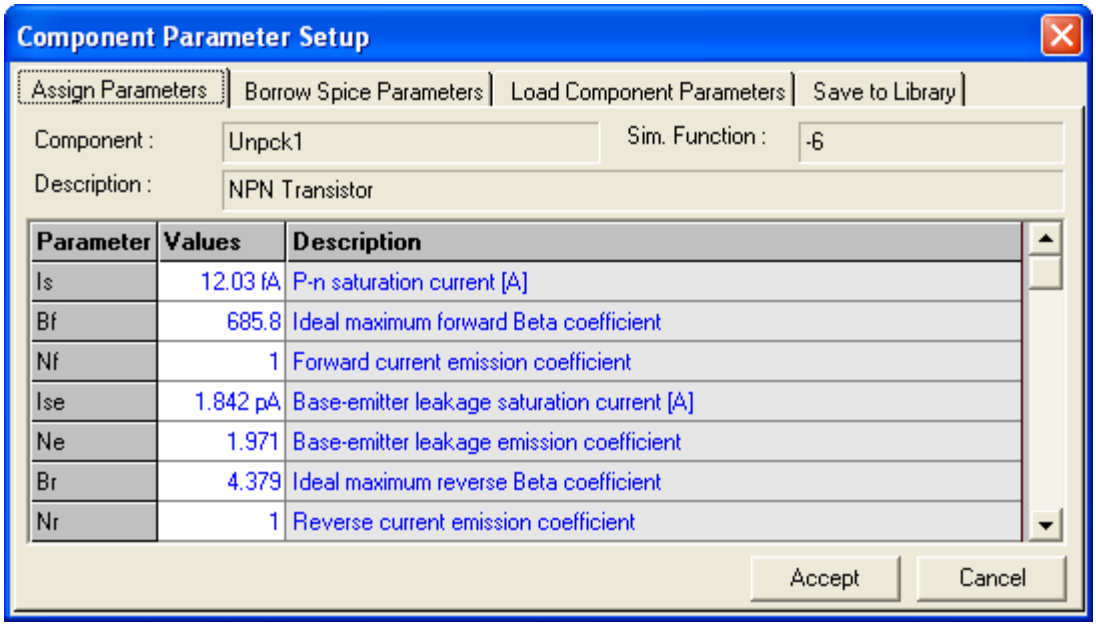


Fig. 6.7

3. After setting the parameters of the circuit, select **Simulation / Analysis**. A window **Setup Simulation Parameters** pops up as shown in the figure.

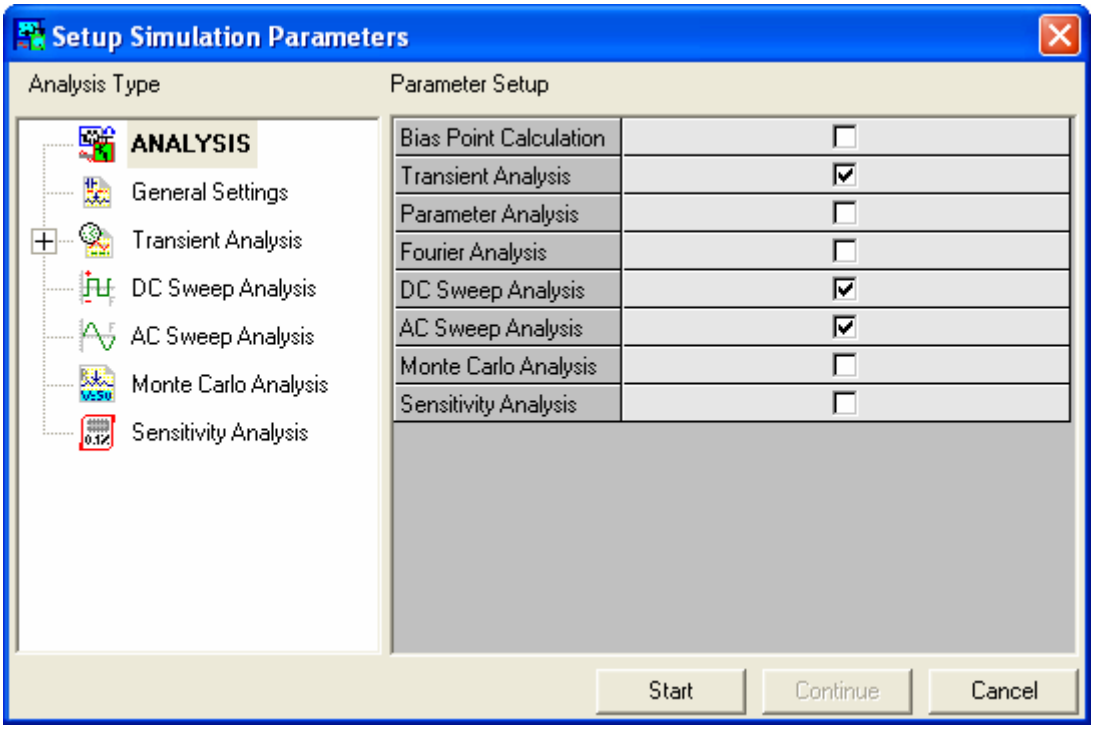


Fig 6.8

Set the parameters by selecting **GENERAL SETTINGS** from the tree view on the left side of the window. Click ***Accept*** button to accept the changes and to automatically switch to Analysis option. Select **Bias Point Calculation** and click the ***START*** button.

You can observe that the node voltages are displayed at the locations where test points were placed. From this we will observe that the operating point of the transistor is found to be near the saturation region. For more details, you can check its Base and Collector currents. Right click and select  **Current TP** option tool from the function tools of  **Test point**. Click on transistor base and collector pins to place the **Current Test point Display** Box.

It is necessary to run Bias Point analysis before any other analysis to set the values of the test points placed.

Transient analysis

In the Transient analysis, we will study the performance of the circuit in time frame.

For example, in **AMPLIF.EPB** the amplifier is fed with an input signal that varies with time in specified manner. Transient Analysis is used to view the input and output with respect to time.

We have analyzed the amplifier small signal properties. At 10 kHz, amplification is 40dB (output amplitude is about 90 times greater than input signal), this means that we can apply max. of about 50mV on input without distortion:

1. We will now define the amplitude of the generator signal. Right click and select the function tool **Component Properties** and then the option tool **Change Simulation Parameter**, click the input generator **VGEN**, the component parameter set up window appears as shown in Fig. 6-9.

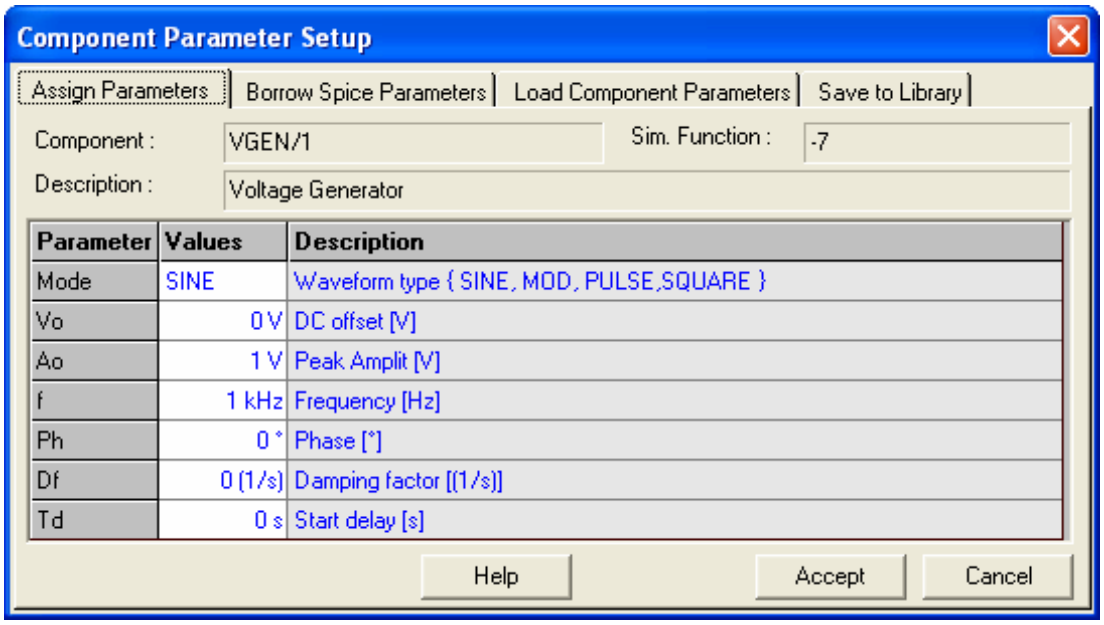


Fig. 6.9

2. The Voltage Generator is in the SINE mode and produces 10mV, 10kHz signal. This would be amplified without distortion. As you found from AC Sweep analysis, the maximum amplitude that may be specified was about 50 mV. Click the ***Accept*** button to save the changes.
3. Right click and select the Delete tool and delete all previously used Waveform Test points.
4. Right click and select the **Voltage Waveform** option tool from the function tool **Set Waveform Contents** and define new Voltage test points on the nets, on generator input (between VGEN and resistance RG), on transistor Base, on transistor Collector and on amplifier load (between C2 and RL).
5. Select the **Current Waveform** option tool from the function tool **Set Waveform Contents** and define new Current test points on the pins: generator "-" pin, transistor collector pin, load resistor RL (upper pin).

6. Click Analysis in the main menu. A window Setup Simulation Parameters opens with the option Analysis being highlighted Set the parameters by selecting **GENERAL SETTINGS**.

7. Select **Transient Analysis**. Specify the timing parameter. Set the Analog Sim. Step time to 1 microsecond, Simulation Time Limit to 200 micro second (two generator periods). Initialize LC parameter should be set to Solve (Refer fig. 6-10).

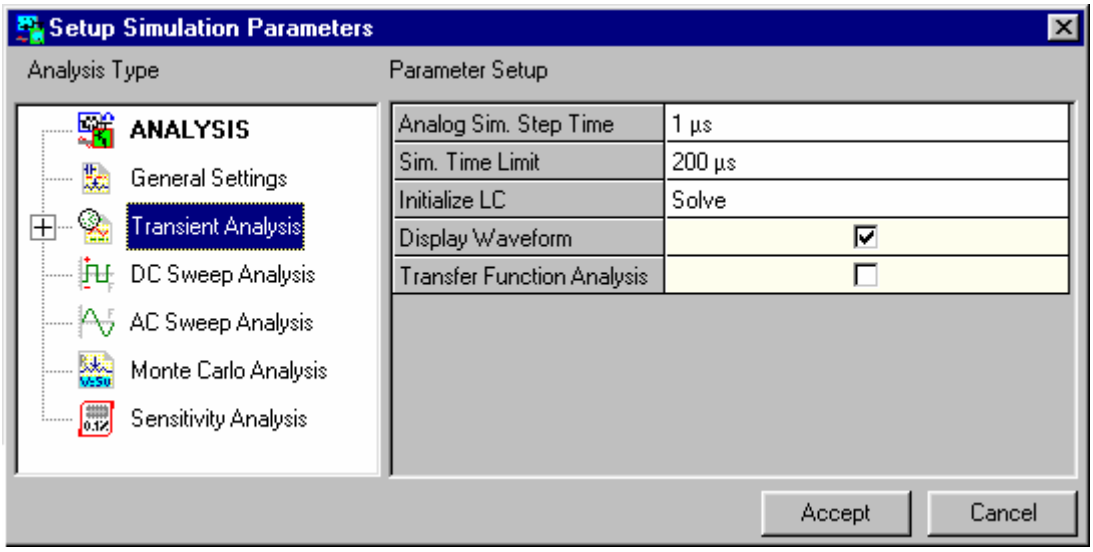


Fig. 6.10

8. Click the ***ACCEPT*** button which automatically switches Analysis option. Here, check **Transient Analysis** and click ***START*** button. The result is displayed as a diagram if Display Waveform is checked.

9. We may change the Generator parameter Ao from 10mV to 100mV and rerun the Transient Analysis. You can view some distortion in the output waveform.

10. Reset the value of Ao to 10mV.

Tips: The result of an analysis can also be viewed in text format (decimal/hexadecimal/binary) with the Logic Analyzer (Simulation/Run Transient Analysis (Logic Analyzer) .The output at any point of time during the simulation can be obtained in word format using this application.

Transient Analysis on Digital circuits

From the **File** menu of the Project Explorer, select **Open Project/ PCB Layout** folder and then open **Counter.EPB** from the file list.

Invoke the mixed mode simulator and execute the preprocessing.
(Refer- Steps for Mixed Mode Simulation Page: 171)

Before starting the Transient Analysis, the circuit state must be initialized. Analog part of the circuit has one state variable: voltage on the capacitor C. We may assume that it starts from the zero value (the power-up condition). This may be achieved by the proper setting of the **Transient Analysis/ Initialize LC** option in the **Setup Simulation Parameters** dialog box invoked from the **Analysis** menu.

1. Initialization of the digital part of the circuit is essential as outputs of the inverters, and output state of the D Flip-flop must be considered. We have to input a Clock pulse to analyze the working of the circuit.
2. Right click and select the option tool **Clock Generator** from the function tool **Preset Logic State** and click on the 7404,1 (U1) and enter the generator string value of (L10us,H10us). This indicates a continuous clock pulse having a 10µs Low and 10µs High pulse width.
3. Enter 5V to the Voltage source from the **Change Simulation Parameters** tool and clicking on the Voltage Source.
4. Place **Logic state marker** on the input node of U1 and on output nodes (Q) of all D-Flip flops using the option tool **Logic Waveform** enabled from the function tool **Set Waveform Contents**
5. Click **Analysis** in the main menu. A window Setup Simulation Parameters opens with the option Analysis being highlighted on the left side of the window by default. Set the parameters by selecting **GENERAL SETTINGS** from the tree view on the left side of the window. Select **Transient Analysis** and set Analog Sim. Step Time to 10 microseconds. Set Simulation Time Limit to 500 microseconds. Set Initialize LC to Solve. Click the ***ACCEPT*** button to automatically switch to the Analysis option and select the ***START*** button to begin the analysis (Refer Fig. 6.11).

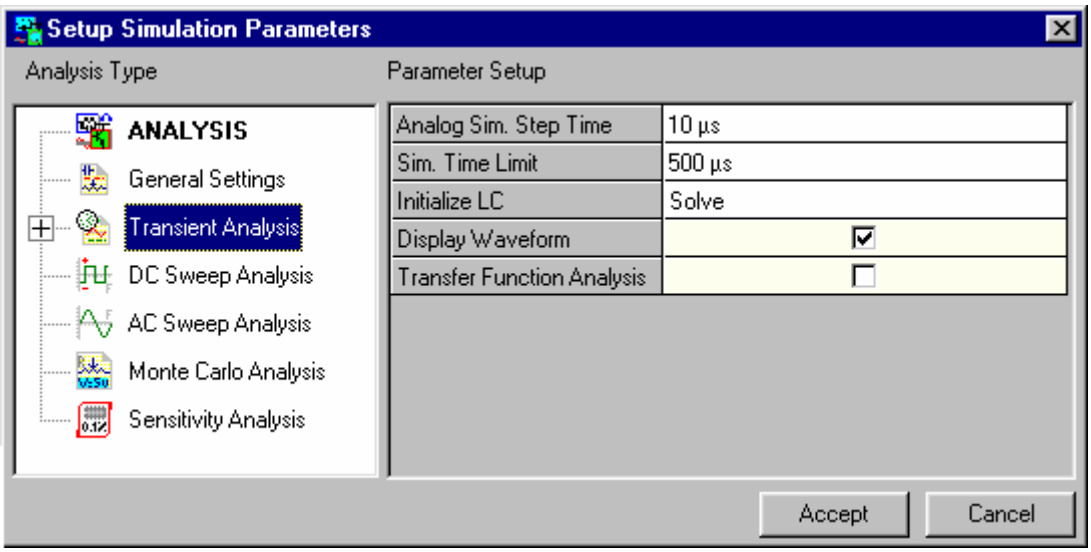


Fig. 6.11

6. After the analysis is completed, the result is displayed as a diagram if Display Waveform is checked. Value of the Analog Simulation Step Time defines time step used in the analog integration process resolving the capacitor voltage. It also defines sampling rate of analog data output to the diagram display module. The shorter the Analog Sim. Step Time, better is the accuracy of analog integration and density of analog graphic results obtained.

Tips: To view the transient analog /digital response of any node or net in the circuit. Select Instant analog probe or Instant digital probe from Instruments/Instant Probes and click on the required node/net. The response that appears in the waveform viewer will be node current or net voltage depending on whether node or net is selected.

Parameter Analysis

This analysis mode allows studying the effect of variation of component parameters on the circuit. This is helpful in setting up the best operating conditions for the design, before detailed functional analysis is made.

1. Right click and select the function tool **Set Waveform Contents** and then the **Voltage Waveform** option tool and define new Voltage test points on the nets, on generator input (between VGEN and resistance RG), on Collector terminal of the transistor and on amplifier load (between C2 and RL).

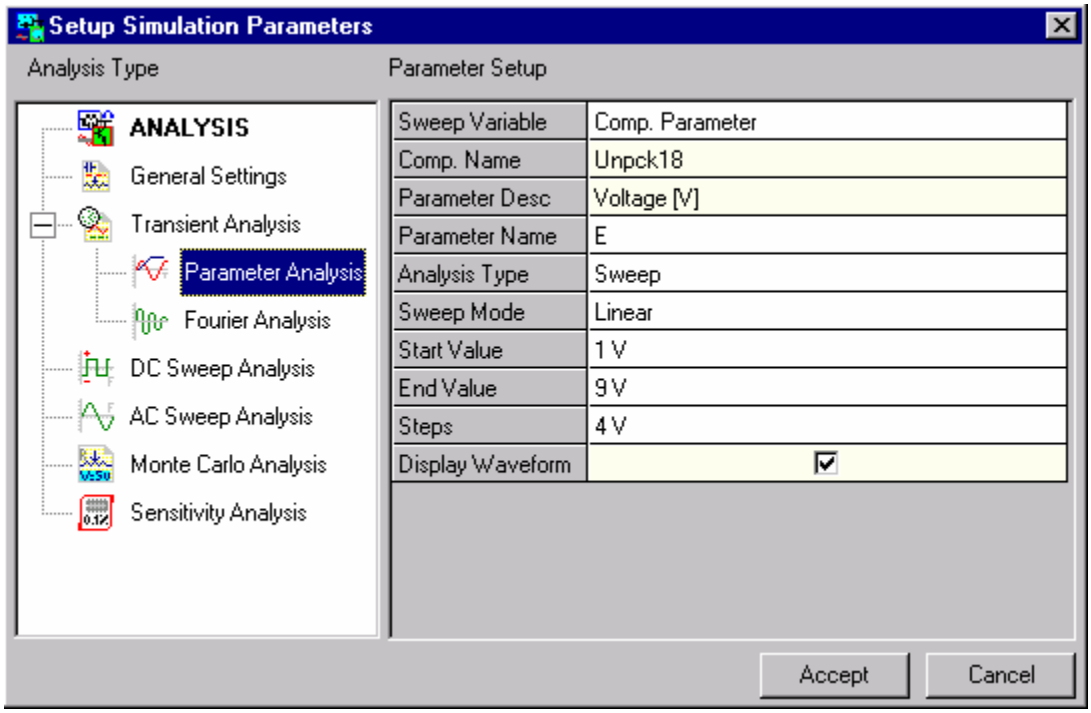


Fig. 6.12

2. Click **Analysis** in the main menu. A window **Setup Simulation Parameters** opens with the option Analysis being highlighted on the left side of the

window by default. Set the parameters by selecting **GENERAL SETTINGS** from the tree view on the left side of the window. Now, select the Parameter Analysis option (Refer Fig. 6-12).

3. Select the Sweep Variable as 'Comp. Parameter'. Move the cursor over Voltage Source and click the left mouse button. The selected component name and parameter name appears in the dialog box. If it has only one parameter, then it is automatically selected. If you have more parameters, you will have to specify the parameter of the component, e.g., a transistor, from the drop down 'Parameter Name'.

4. Set the values for the following parameter as shown below.

Start Value	1V
End Value	9V
Step	4V

5. Click ***ACCEPT*** button to automatically switch to Analysis option. Check Parameter Analysis check box. Now click START button for analysis to take place. The results may be viewed in the Waveform Viewer and the most suitable parameter value may be obtained.

Fourier Analysis

This analysis is used to calculate the total harmonic distortion of analog waveforms generated on conducting transient analysis.

1. We will check the harmonics of the waveform generated on conducting Transient analysis of **AMPLIF.EPB**.

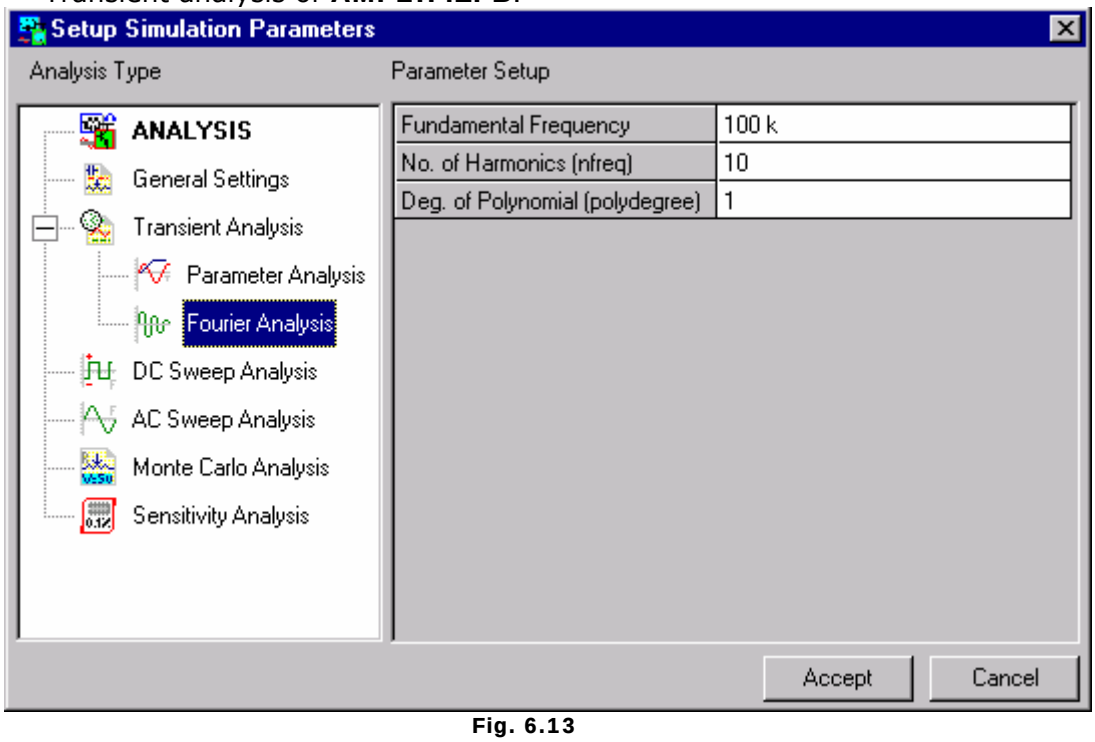


Fig. 6.13

2. Select Analysis from the main menu to open Setup Simulation Parameter with the option Analysis being highlighted on the left side of the window by default. Set the general parameters and select **Fourier Analysis** from the tree view or obtained on right clicking **Analysis**.

3. The parameters to be set are the fundamental frequency of the waveform whose distortion is being computed. Set it as 100KHz. No. of harmonics as 10 and the degree of polynomial to be 1 (Refer Fig. 6.13).

4. After setting these parameters, click the ***ACCEPT*** button to accept the parameters and automatically switch to Analysis option. Check Fourier analysis. The ***START*** button executes the analysis and displays the process in the Progress bar.

5. The results are displayed in a text format.

DC Sweep Analysis

DC Sweep Analysis: Bias Point Setup

Let us examine the effect of the circuit AMPLIF.EPB modifying the value of RB2 on the operating condition of the circuit. We will vary the value of RB2 from say, 5K to 20K in steps of 0.5K and observe the circuit operating parameters. We would like to present the results in a graphical form to assess the correct value for RB2. The parameters of concern for this analysis are Vce, Ib and Ic. As we need graphical representation, we will have to define these points.

1. Right click and select the  **Voltage Waveform** option tool from the function tool  **Set Waveform Contents.** Define Voltage Waveform Marker for Collector voltage by clicking on the wire connected to the transistor Collector pin. In the same way, define for Emitter voltage.
2. Right click and select the  **Current Waveform** option tool from the function tool  **Set Waveform Contents**. Define Current Waveform Marker for Base current by clicking on the transistor Base pin. In the same way, define for Collector current.
3. Click **Analysis** in the main menu. A window Setup Simulation Parameters opens with the option Analysis being highlighted on the left side of the window by default. Set the parameters by selecting **GENERAL SETTINGS** from the tree view on the left side of the window. Now, select the DC Sweep Analysis option (Refer Fig. 6.14).

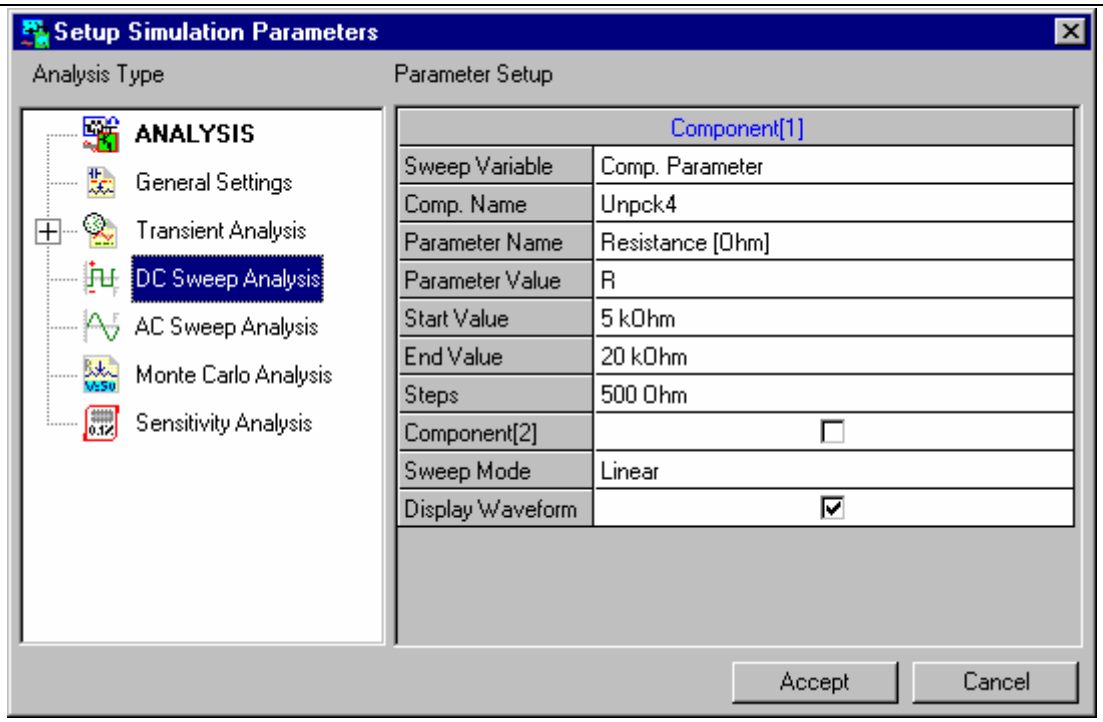


Fig. 6.14

4. We will first select the **Sweep Variable as Comp. Parameter** in this dialog box. Move the cursor over the resistor RB2 and click the left mouse button. The selected component name and parameter name appears in the dialog box. Selected resistor has only one parameter, and is automatically selected. If we have more parameters, we will have to specify the parameter of the component, e.g., a transistor, from the drop down '**Parameter Value**'. We may conduct the analysis when the parameter of one circuit element is varied keeping the parameter of another circuit element constant, through out a range of values. In that case, check the check box Component (2) and set its parameters.

5. We will now set the sweep limits for RB2, enter 5k in the Start value box, and 20k in the End value edit box. As the range is limited for sweep, we can choose Linear and enter 0.5k in the Step edit box. This completes the parameter setting. We can enable the check box next to Display waveform, if we want the system to automatically pop up the display waveform. We will not select this for the current exercise. Click ***ACCEPT*** button to automatically switch to Analysis option. Check **DC Sweep Analysis** check box. Now click ***START*** button for analysis to take place.

6. During the simulation, we may observe the results as they occur in each step. To choose the best bias point result depended on the setting of the resistor RB2, we will use the graphical results of the simulation.

7. The **Waveform Viewer** (enabled automatically if Display waveform is checked.) application window appears showing four curves as results of the analysis. These curves show the waveforms defined earlier, viz. V1 (Collector), V2 (Emitter), I1 (Base) and I2 (Collector). From these waveforms,

we must solve a little problem. Find the RB2 value for which Ic/Ib = Beta (approx.) and Vc-Ve is about half of Vcc-Ve.

8. Close the **Waveform Viewer**.

9. We will now modify the value of RB2 to the value arrived at after the analysis. Select the function tool **Component Properties** and then select the option tool **Change Simulation Parameter** to update the component value for RB2. Click the left mouse button on the RB2 resistor. Click the cell under the value column. Enter the new value (11kΩ into the editable text box at the current location) in the appeared Assign Parameter For dialog box (Refer Fig. 6-15).

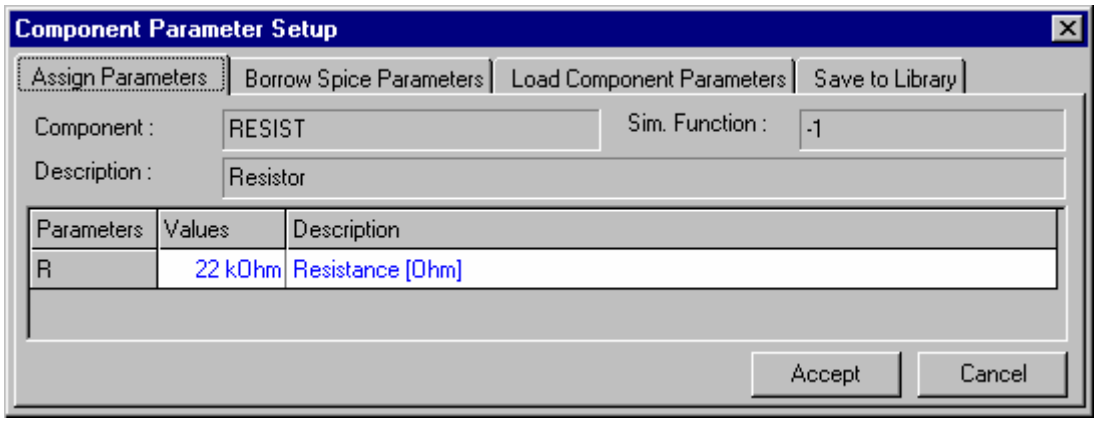


Fig. 6.15

10. Click the ***ACCEPT*** button. We will observe the new value for RB2 on the simulation screen.

11. We will recompute the bias points to ensure that the transistor operating condition is just right. From main menu choose Analysis. Check **DC Sweep Analysis** check box. Now click ***START*** button for analysis to take place. Verify the results.

DC Sweep Analysis: Transistor Beta Bf

We will try out DC Sweep analysis for checking circuit sensitivity when the transistor parameter Beta (Bf) changes from 100 to 400.

1. Click **Analysis** in the main menu. A window **Setup Simulation Parameters** opens with the option Analysis being highlighted on the left side of the window by default. Set the parameters by selecting **GENERAL SETTINGS** from the tree view on the left side of the window. Now, select the **DC Sweep Analysis** option. Move the cursor over the transistor and click the left mouse button.

2. As the transistor has more than one parameter, all parameters are listed in a drop down defined for the component. Here, select the Bf parameter from the Parameter Value drop down in the Setup Simulation Parameters dialog box.

3. Define the sweep limits as 100 for the Start value edit box and 400 for the End value. Select the **Sweep mode** to be Linear and enter 20 in the Step cell. Click the ***ACCEPT*** button.

4. In the Progress display area, current iteration status (iteration number and voltage errors) is displayed continuously. We may disable this option and speed up the simulation. For this, select the General Settings option in the Setup Simulation Parameters dialog box that appears when Analysis is clicked in the main menu. Change selection of the check box named **Display Iteration Errors**. Click the ***ACCEPT*** button.

5. We may also disable the **Display TP values** check box in **General Setting's** option to obtain the fastest simulation run. Results may be reviewed in the Waveform Viewer only.

DC Sweep Analysis: Operating Temperature

We may also sweep the ambient temperature and observe the circuit response:

1. Click **Analysis** in the main menu. A window Setup Simulation Parameters opens with the option Analysis being highlighted on the left side of the window by default. Set the parameters by selecting GENERAL SETTINGS from the tree view on the left side of the window. Now, select the DC Sweep Analysis option.

2. Select the **Sweep Variable as Temperature.**

3. Define the sweep limits as -30 for the Start value edit box and 100 for the End value. Select the Sweep Mode to be Linear and enter 5 in the Step box. Click the ***ACCEPT*** button.

4. Observe the results in the Waveform Viewer, after checking **Display Waveform** check box in the **Setup Simulation Parameters** dialog box.

AC Sweep Analysis

The circuit operating parameters have all been stabilized for the circuit AMPLIF.EPB and set after the DC sweep analysis. Now we may calculate the small-signal frequency response of the circuit assuming its current biasing. We will not define any AC parameters for the active components like transistor - the Simulator assumes their values calculated internally from the nonlinear transistor model using its operating point.

1. Before any further analysis is performed, compute the operating point again, using Analysis menu (Refer- Bias Point Calculation Page - 174).
2. We will now have to define the AC Analysis input points. Right click and select the  AC IN+ option tool from the function tool  Set Reference Points. Click the left mouse button at the "+" terminal of the Generator. We will see a text "IN+", position this AC Input test point.
3. To define the AC Analysis output points, right click and select the  AC OUT+ option tool from the function tool  Set Reference Points. Click the left mouse button on the net connected between C2 and RL. We will see a text "OUT+", position this AC output test point.
4. The AC test points IN- and OUT-, for AC input and output are by default assigned to ground net SPL0 and we need not define them except for special cases.
5. We will now have to define the frequency sweep parameters. Click Analysis in the main menu. A window Setup Simulation Parameters opens with the option Analysis being highlighted on the left side of the window by default. Set the parameters by selecting GENERAL SETTINGS from the tree view on the left side of the window. Now, select the AC Sweep Analysis option (Refer Fig. 6-16).

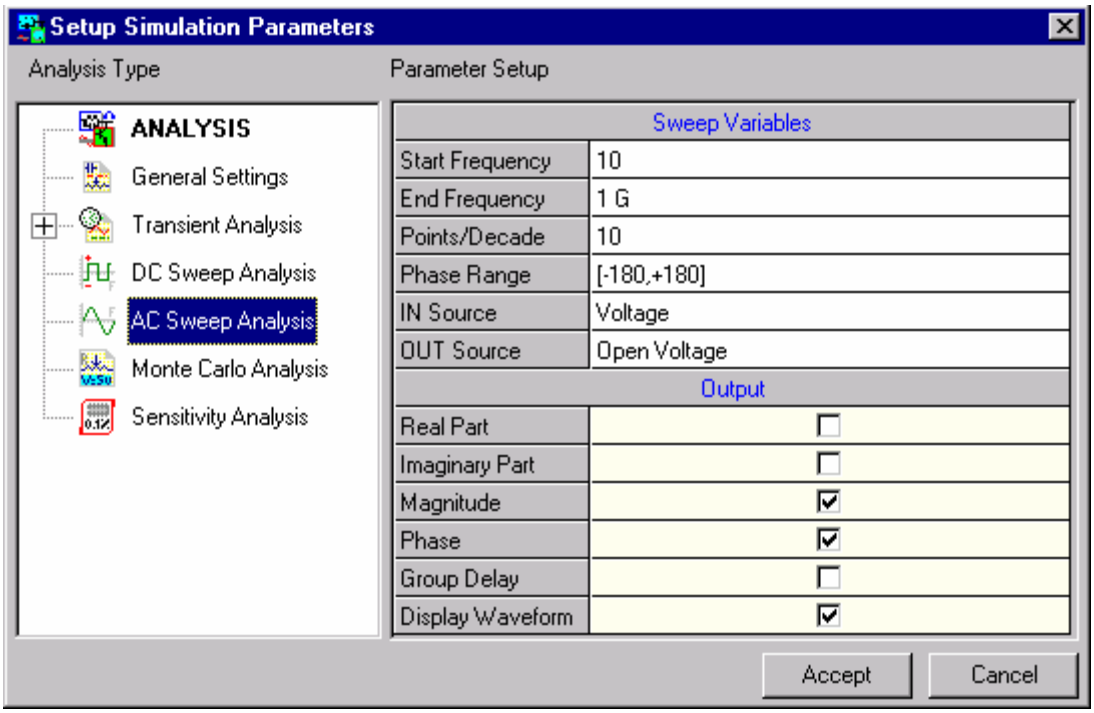


Fig. 6.16

Set the values for the following parameter as shown below.

Start Frequency	10 Hz
End Frequency	1 GHz
Points per Decade	10
Range of Phase	[-180°, +180°]
IN source	Voltage
OUT variable	Open voltage
Output	Magnitude, Phase, Group Delay.

6. We will observe that the AC simulation will analyze the circuit response for a frequency sweep from 10 Hz to 1 GHz (8 decades) with 10 points per decade - total 81 points. Phase shift is calculated within the range from -180° to +180°. An AC voltage input source is placed between IN+ and IN- net. An AC voltage is measured on the opened OUT+ and OUT- nets. The ratio Vout / Vin will be an output that is shown in three forms: magnitude, phase and group delay.

7. Click ***ACCEPT*** button to automatically switch to Analysis option. Check AC Sweep Analysis check box. Now click ***START*** button for AC Simulation Pass to take place.

8. If Display Waveform is checked in the above dialog box, the output is displayed in the Waveform Viewer and the three curves depict the graphical dependency of the calculated Gain, Phase Shift and Group Delay from the frequency parameter. From this, we see that the lower unity-gain frequency is about 60 Hz, upper unity-gain frequency is about 50 MHz. Middle-frequency gain is about 40 dB.

We will save the results by Selecting **File | Save** in the Waveform Viewer menu. Specify the name of the file and click **OK**. Exit from the Waveform Viewer.

We can now test the circuit AC characteristics for another bias point. For example, with the RB2 set to its original value 20k ohms do the following.

1. Right click and select the  **Component Properties** and then select the option tool  **Change Simulation Parameter** and set RB2 resistor to 20k value.

2. Click **Analysis** in the main menu and select the Analysis from the Setup Simulation Parameters dialog box that appears. Enable the Bias Point Calculation check box in order to recompute the bias point for the design.

3. Enable **AC Sweep Analysis** check box after selecting the Analysis option in the Setup Simulation Parameters dialog box. Click the **ACCEPT** button to start the AC analysis.

4. Display the **AC Sweep** diagram.

5. We see that unity-gain frequencies are now 180 Hz and 500 kHz, and the maximal gain is now about 24 dB. The original bias point gives a poor AC circuit response.

Monte Carlo Analysis

It is used to calculate accurate component parameter values for a given output at a given instant of time. We will study the performance of the circuit **AMPLIF.EPB**.

1. Right click and select the  Monte Carlo Voltage option tool from the function tool  Set Reference Points. Define the reference point by clicking on the wire connected to the transistor Collector pin.

2. Click Analysis in the main menu. A window Setup Simulation Parameters opens with the option Analysis being highlighted on the left side of the window by default. Set the parameters by selecting GENERAL SETTINGS from the tree view on the left side of the window. Now, select the Monte Carlo Analysis option.

3. We will select the Component RB1. Move the cursor over the resistor RB1 and click the left mouse button. The selected component name and parameter name appears in the dialog box. Selected resistor has only one parameter, and is automatically selected. If we have more parameters, we will have to specify the parameter of the component, e.g., a transistor, from the drop down 'Parameter Value'. We may conduct the analysis when the parameter of one circuit element is varied keeping the parameter of another circuit element constant, through out a range of values. In that case, check the check box Component (2) and set its parameters.

4. Set the Tolerance to be 10% and No. of samples 10. Tolerance specifies the percentage range of variation of component parameters. No. of Samples specifies the number of iterations within the output range for which analysis is to be carried out. Time specifies an instant of time at which the accurate parameter value is to be calculated for obtaining the specified output. Set it as 10ms (Refer Fig. 6-17).

5. Click ***ACCEPT*** button to automatically switch to Analysis option. Check Monte Carlo Analysis check box. Now click ***START*** button for analysis to take place.

6. The results are displayed in a text file.

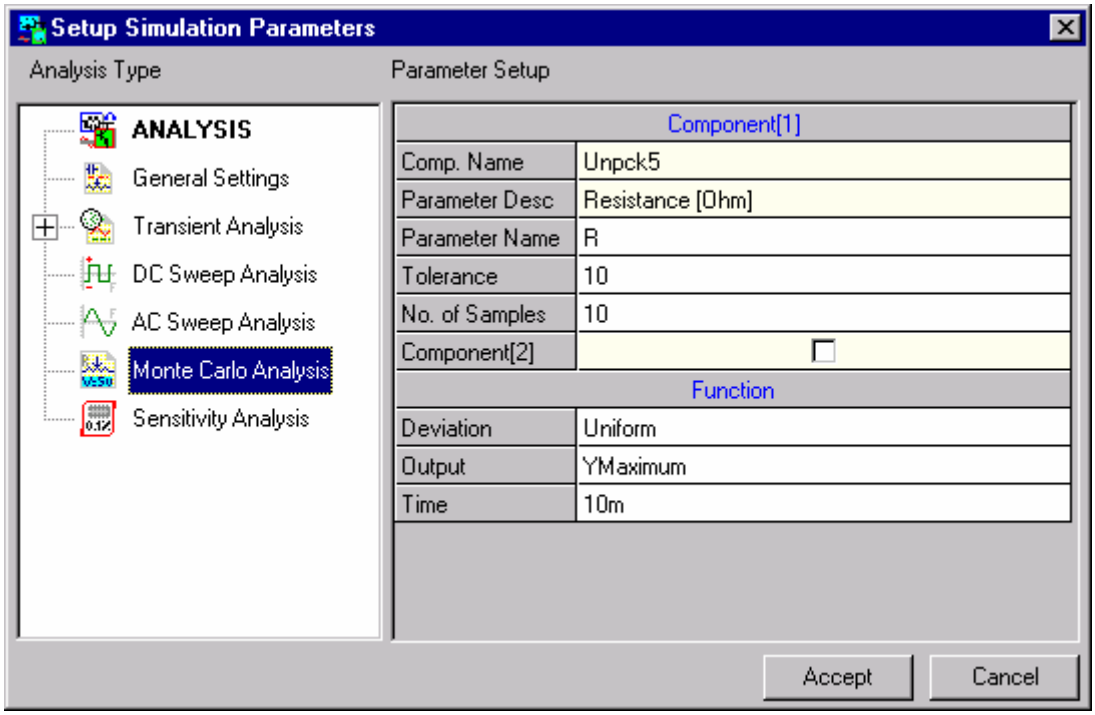


Fig. 6-17

Sensitivity Analysis

It is used to calculate the component that is most sensitive to an output reference point. Please refer **AMPLIF.EPB** to study the performance of the circuit.

1. Right click and select the  **Sensitivity Voltage** option tool from the function tool  **Set Reference Points**. Define the reference point by clicking on the wire connected to the transistor Collector pin.
2. Click **Analysis** in the main menu. A window Setup Simulation Parameters opens with the option Analysis being highlighted on the left side of the window by default. Set the parameters by selecting **GENERAL SETTINGS** from the tree view on the left side of the window. Now, select the Sensitivity Analysis option (Refer Fig.6-18).

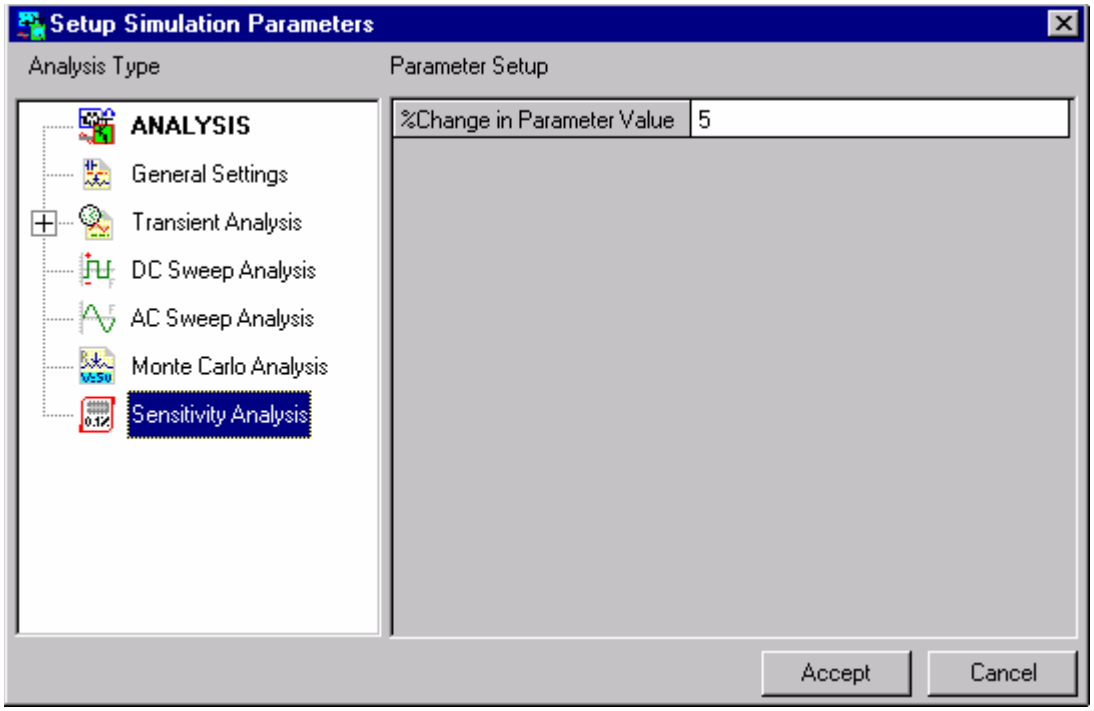


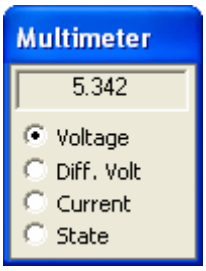
Fig. 6.18

3. Specify a 5% of tolerance for which the analysis is to be carried out. This is the common tolerance value for all parameters of all components.

4. Click ***ACCEPT*** button to automatically switch to Analysis option. Check Sensitivity Analysis check box. Now click ***START*** button for analysis to take place.

5. The results are displayed in a text file. The most sensitive component and its parameter is listed as the last line of the text file.

Tips: Use Multimeter from Instruments/ Test Points and click on the net or node to view the voltage, current and logic states of selected net or node in the circuit after simulation.



How to simulate Microcontrollers?

For a component to be simulated in Mixed Mode simulator, it should have a corresponding primitive, which will contain information about its behavioral characteristics, which the simulator uses to construct the final output. The system has primitives for 8051, AVR, PIC and Motorola microcontrollers therefore it is

possible to simulate these if there is an associated binary file of the Assembly language program. The binary file may be assigned to the microcontroller as follows. Select Change simulation Parameters (Second Option tool) from Tools/Components/Component Properties (Second function tool)/ and click on the microcontroller, a window appears as shown below, click on Setup to view the Setup window.

The Binary file can be imported to EDWinXP using Import Options in Hex Editor [ROM] or can be generated using C/Assembly Editor in Setup Window.

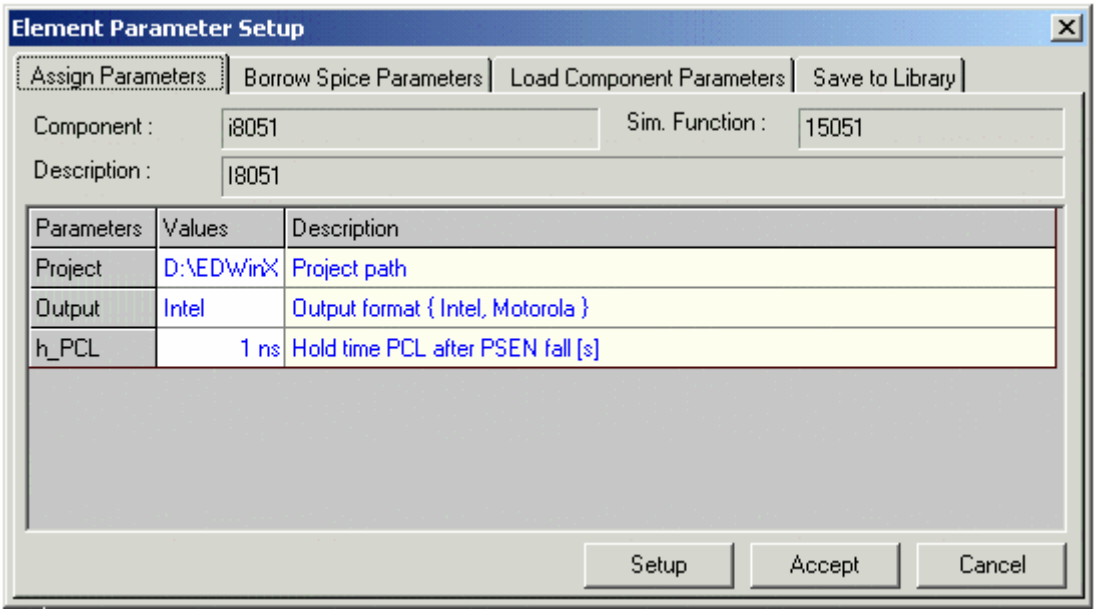


Fig.6.19

Setup

On clicking the ***SETUP*** button of Component Parameter dialog of the required model, the MMI window appears as shown in Fig.6.20.

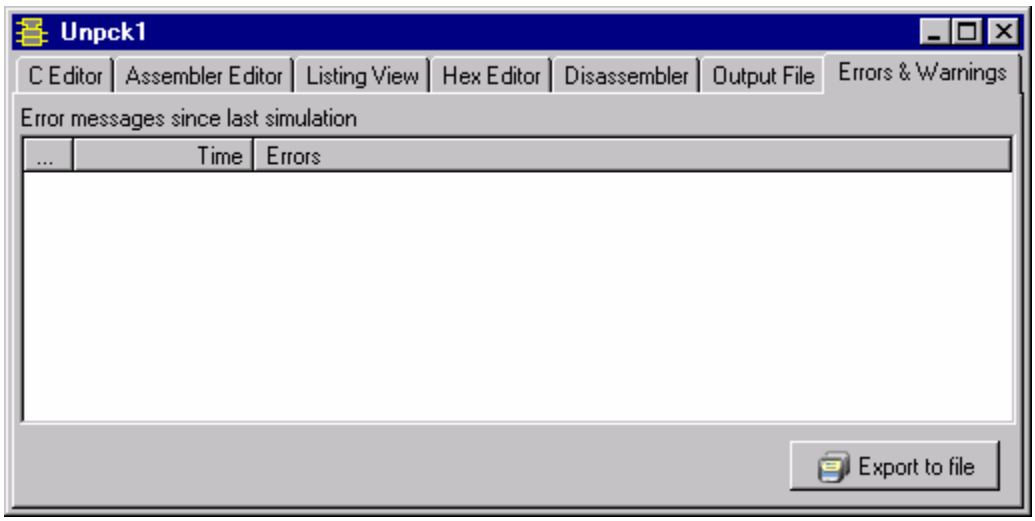


Fig.6.20

C Editor

If you intend to code the program in C, select the **C Editor** tab.

The different options of the C EDITOR are explained below

Clear text

The clear option helps the user to clear the context of the code editor

Import

The import option enables the user to display the Open Dialog Box to input file name and loads the text file from the disk.

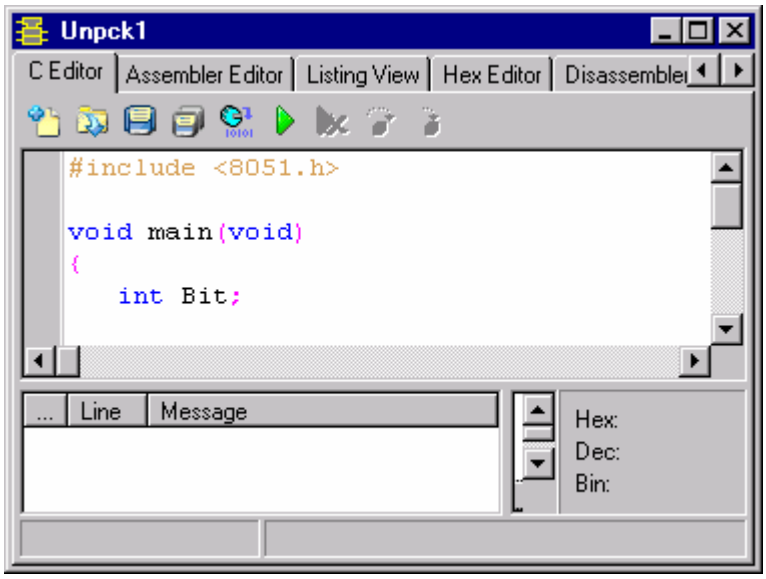


Fig.6.21

Save

The save option Generates an On Save event to notify model to save the source code in the internal file of the associated simulation component.

Export
The export option displays the On Save Dialog Box to prompt the user for output file name and saves the source code to the disk.

Compile
The compile option enables the user to Generate an On Compile event to notify model to compile the source code.

Build
The build option Generates an On Build event to notify model to compile the source code.

Start Debug
The debug option helps the user to Generate an On Debug event to notify model to debug the source code.

Stop Debug
This option allows the user to stop debugging which is associated with the generation of an On Stop debug event to notify model to stop debugging the source code.

Step Over
The option allows the user to Generate an On Step Over event to notify model to step over the being currently debugged part of code.

Trace Into
The option allows the user to Generate an On Trace Into event to notify model to trace into the being currently debugged part of code.

Assembler Editor

If you intend to code the program in Assembly Language, select the tab Assembler Editor.

Listing View

Listing view represents the listing format of assembler code.
After the compilation is done, Listing view window will present the next information i.e.

1. Real addresses of all assembler instructions used in the code.
2. Real (physical) addresses of all data in the code scope.
3. Real addresses of global variables which use the internal memory of microcontroller.
4. The initial address of stack pointer.
5. Information about used banks of registers.

You may require this information for further debugging and optimization of the source code.

Hex Editor

The Hex Editor Sheet is used to display the binary data in either Hex or ASCII formats. Also it allows to edit the binary data and provides the import and export functions.

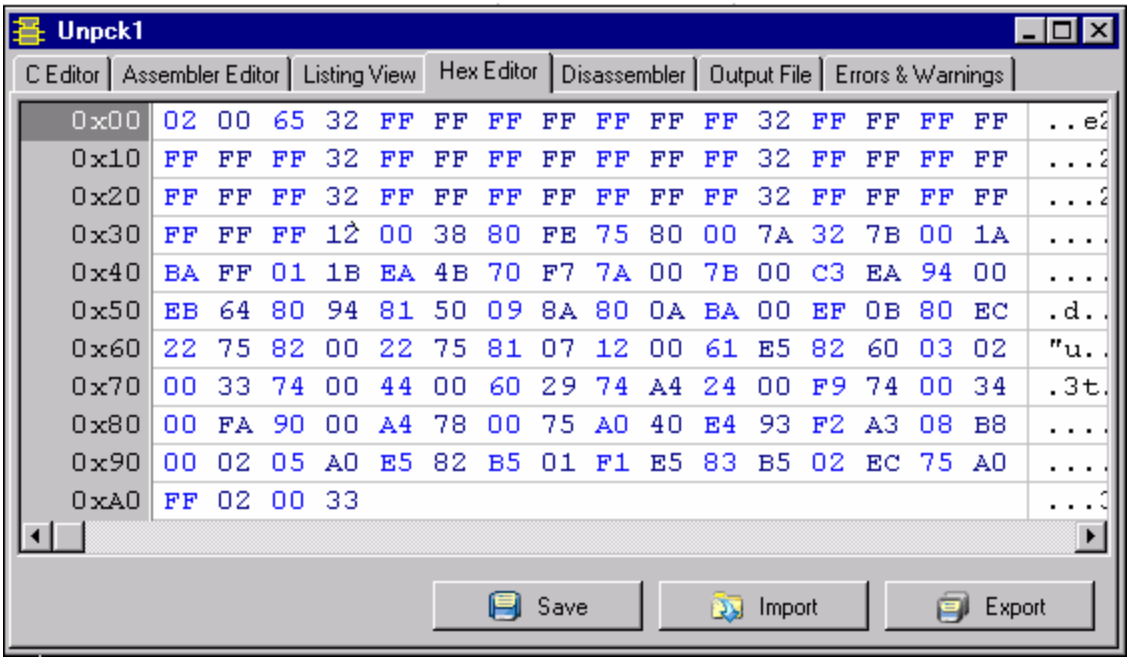


Fig.6.22

Options available in Hex Editor Sheet are:

Import	Allows to save binary data to the disk.
Export	Allows to load binary data from the disk.
Save	Generates an event to notify model that user wants the binary data to be saved in the internal file.

Disassembler

In the Disassembler window user may see the continuous address area. It reflects the instructions really loaded to the microcontroller including the library functions.

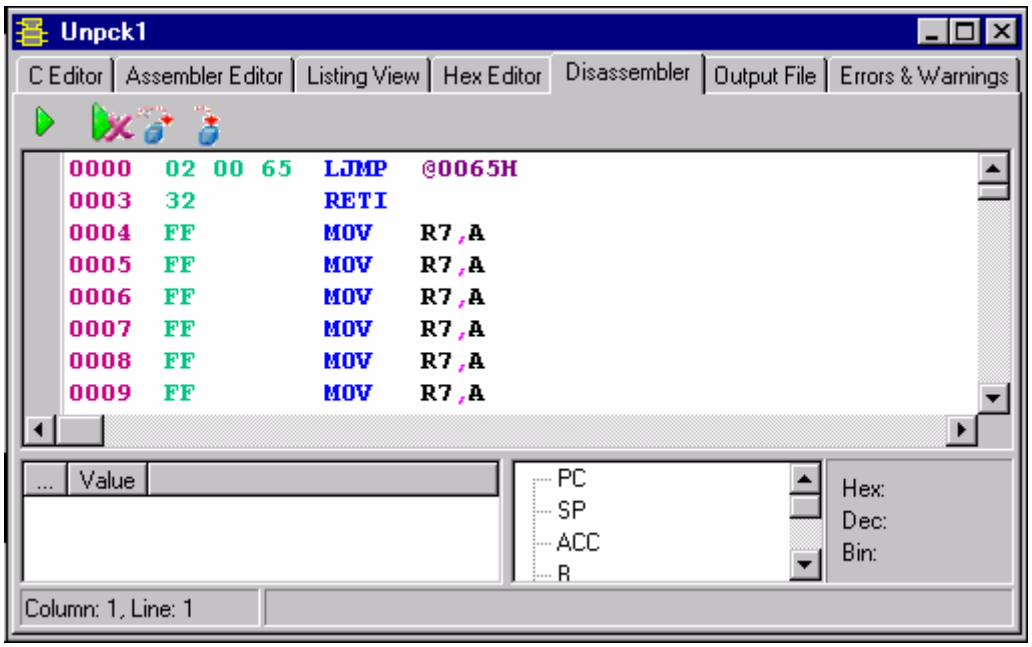


Fig.6.23

Output File

The output file generates the binary code of the program written in the C EDITOR. The output file has an option **EXPORT TO FILE**. The Export To File option displays the Save Dialog Box to prompt the user for output file name and saves the source code to the disk.

Errors and warnings

The Errors and Warning displays the error, warning and comment messages generated by the Mixed-mode Simulator during the Time-Domain simulation. Along with text messages (by default they are Error, Warning and Comment, though any kind of messages may be displayed), it also displays the simulation time at which the message has been generated.

There is only one function defined in Error Messages Sheet. It is Export To File. This function allows to save the displayed data to the disk.

The Error Messages Sheet doesn't generate any events.

Chapter 7

EDSpice Simulator

The EDSpice Simulator, which is similar to Mixed Mode Simulator, provides the facility to analyze and validate the functionality and behavior of circuits.
The interactive module of EDSpice provides seamless integration between the simulator and the rest of the system. The core of the package is the EDSpice Simulation Engine, which performs the simulations and outputs the results.
This module includes a set of function tools to prepare circuits for simulation, initiate the execution of analyses, and review the results graphically for textually.

Steps for EDSpice Simulation

Evoke EDSpice Simulator

Circuit simulation starts with invoking the interactive module of EDSpice Simulator from Schematic Editor/ Preference. The user interface is similar to other EDWinXP applications. The schematic diagram of a circuit may be either created or an existing project can be opened from the project explorer window. The same rules govern the selection and interaction with database objects (schematic components and nets) and these objects are referred to as circuit elements and nodes, respectively, according to SPICE conventions.

Preprocess the circuit
The circuit is preprocessed before simulating and is invoked from Simulation menu. Preprocessing confirms whether the circuit is ready for simulation. It should be performed at all times, when elements have been added or deleted from the circuit or connectivity between them is changed.


In the case of a newly captured circuit, the setup of instance and model parameters of the elements must be defined before any simulation is executed.

Set initial conditions for Simulation
Certain global parameters, preset options and conditions for analyses are passed to the simulation engine in the netlist. Dialog windows for defining the contents, lines such as OPTIONS (Simulator variables), .IC (Initial Condition) and .NODESET (Initial Node Voltage Guesses) may be accessed from the Setup dropdown menu.

Run Analysis
The simulation process is initiated by selecting one of the available analyses, setting up the required parameters, and starting its execution. When the selected analysis is executed, the interactive module extracts a SPICE netlist, stores it in a file called EDSPICE.CIR, and a group of commands are passed to the simulation engine. The set of commands that the interactive module passes to the simulation engine depends on the type of analysis, required contents of the results and the form in which the results are to be displayed.

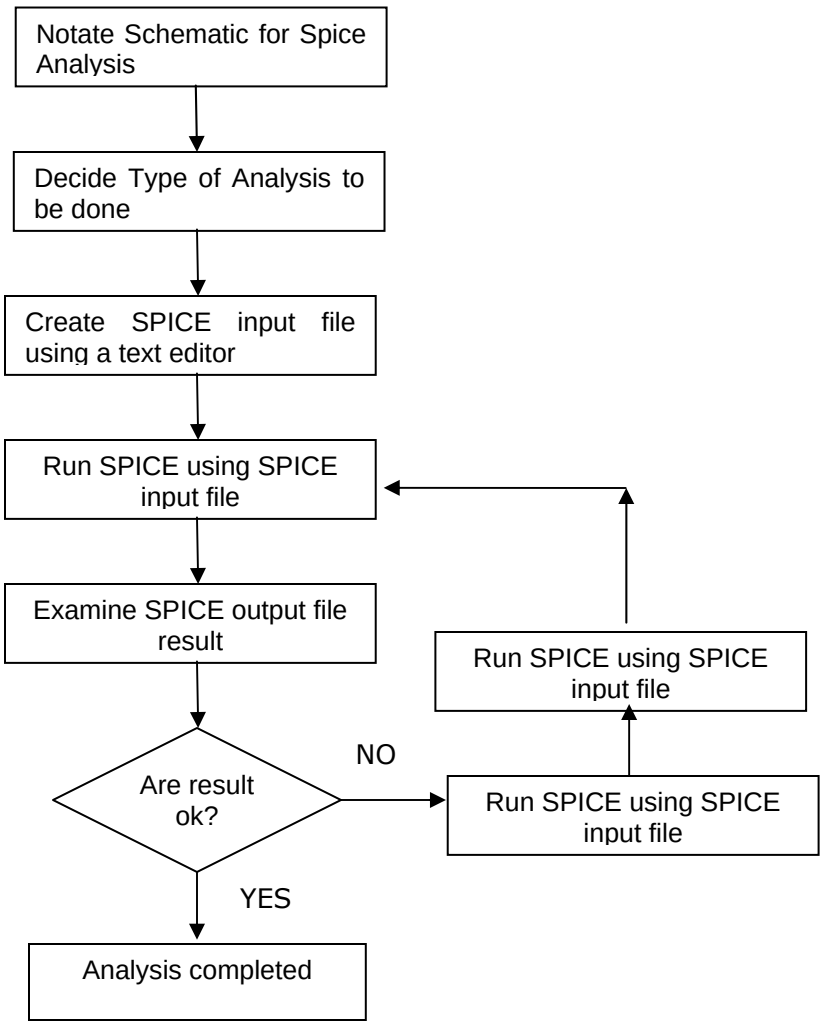
The SPICE netlist of the circuit can be viewed from Options | View EDSpice Files ... | Circuit (SPICE Netlist).
After the commands are received, the simulation engine parses the netlist generated by the interactive module, executes the selected analysis and stores the results in the output files RAWSPICE.RAW and EDSPICE.OUT.

Result of analysis
When the interactive module gets confirmation that the simulator engine has completed the analysis, the results of simulation are processed for presentation. When the whole process is completed the results are displayed in graphical or textual form.

SPICE Simulation

The circuit is represented in the form of a text file called 'circuit file' (.CIR file). This file can be created using any text editor and submitted to SPICE (Simulation Program with Integrated Circuit Emphasis) for analysis.

Steps for using SPICE



1. Start with the schematic diagram and notate it for SPICE consisting of three steps:

   - Name component or circuit element
   - Assign a node (a point of connection between two or more circuit elements) as node zero. This is the ground node, and all other circuit node voltages will be expressed with respect to this node.
   - Each additional node in the circuit is given a node number, which must be a positive integer. The order in which the nodes are numbered is arbitrary, and node numbers need not be sequential. Each node must be connected to at least two elements.

2. Decide the type of analysis. SPICE can do DC, AC, Transient, DC transfer function, DC small-signal sensitivity, distortion, noise and Fourier analyses. Based on the types of analyses, one or more control lines have to be added to the input file. A control line could specify the values of DC voltage or current for a source, range of frequencies an ac source is to have, or the time interval over which a transient analysis is to take place and the time step size to be used

3. Create an input file for SPICE using a text editor. Use only capital letters, the first line must be a title line and it should end with '.END'.

4. Execute the analysis.

Circuit File Editor

The circuit file (.CIR file) describes the circuitry to be analyzed in a format that the SPICE simulation engine can interpret.

Invoke Circuit File Editor, from **Simulation | Circuit File Editor** of EDSpice Simulator.

To perform simulation, follow the steps mentioned below:

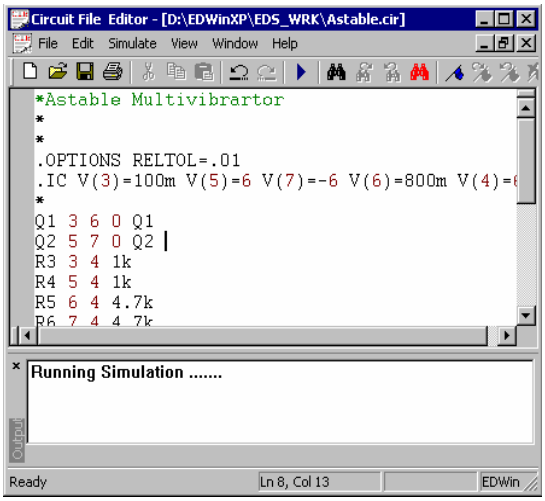


Fig. 7.2

1. Click on File | New.
2. A new window pops up within Circuit File Editor. Paste the circuit file information in this window. Save the information with a suitable name by clicking File | Save.

3. To simulate, click on menu Simulate.

4. The output of simulation is displayed in Waveform Viewer.

The circuit file of Astable Multivibrator and its output are shown below (Fig 7.3)

Circuit File
*Astable Multivibrartor

```
.OPTIONS RELTOL=.01
.IC     V(3)=100m     V(5)=6     V(7)=-6
V(6)=800m V(4)=6

Q1 3 6 0 Q1
Q2 5 7 0 Q2
R3 3 4 1k
R4 5 4 1k
R5 6 4 4.7k
R6 7 4 4.7k
C7 3 7 4.7U
C8 5 6 4.7U
V9 4 0 DC 6

.MODEL Q1 NPN CJE=1p TF=10n CJC=1p
.MODEL Q2 NPN CJE=1p TF=10n CJC=1p

*CODE MODEL DEFINITIONS
.TRAN 10U 100M
.SAVE V(7)  V(5)
.SAVE V (3) V (6)
.END
```

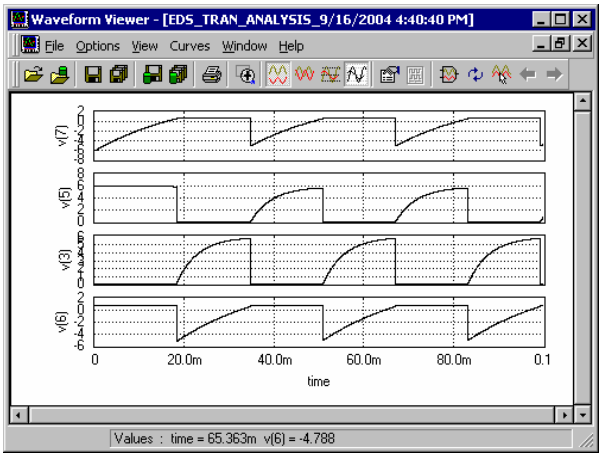


Fig 7.3

EDSpice Interactive Interpreter

This dialog is displayed when **Simulation | Analysis |EDSpice Interactive Interpreter** is selected. In this case, this window is as shown in figure 7.4 and displays details of the simulation.
This may also be invoked directly from a SPICE netlist of *.CIR format without creating the Schematic.

Writing a .CIR file –

EDSpice | Simulation | EDSpice Interactive interpreter | New/Edit Circuit | File | New.

Tips: You may also use Windows Notepad for writing .cir file

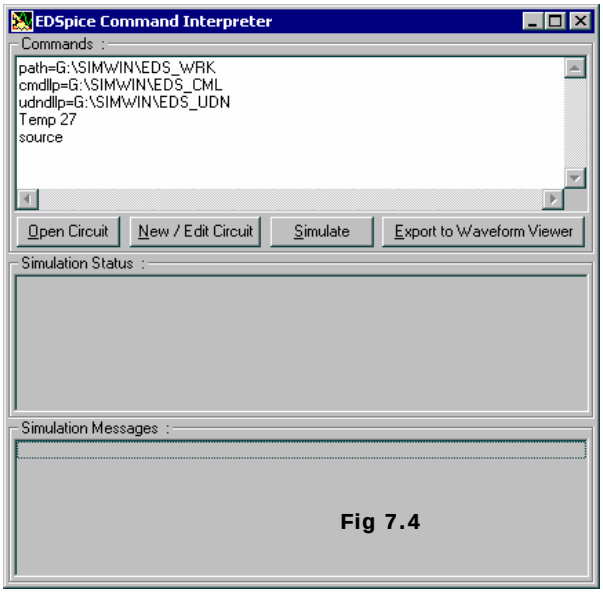


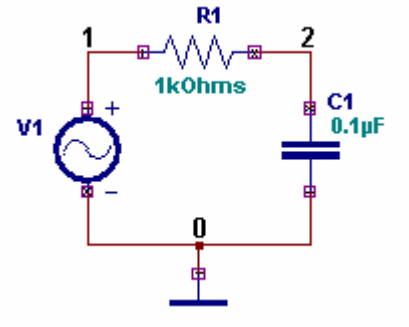
Fig 7.4

Any input file for SPICE should contain

1. a title line
2. element lines for each element in the schematic.
3. a .END line

The following example shows the circuit file for an RC Integrator and to plot its Transient simulated output:

```
* Title line
Integrator.cir
* Element line for each element
* Voltage Source description
V1 0 1 AC PULSE (0 5 0 0 0 .5m 1m
)
C1 2 0 100n
R1 1 2 1k
* Transient Analysis
.TRAN 1µ 5m
* Save results for Waveform Viewer
.SAVE V(1) V(2)
* .End line
.END
```



Simulating a .CIR file

EDSpice | Simulation | EDSpice Interactive interpreter | Open Circuit | Select the .cir file | Simulate.

If .SAVE option is not given in the cir file, then the simulator outputs the simulation results to 'rawspice.raw'. Click on Export to Waveform Viewer and then select the rawspice.raw file to display the outputs in Waveform Viewer. (Refer Fig.7.5)

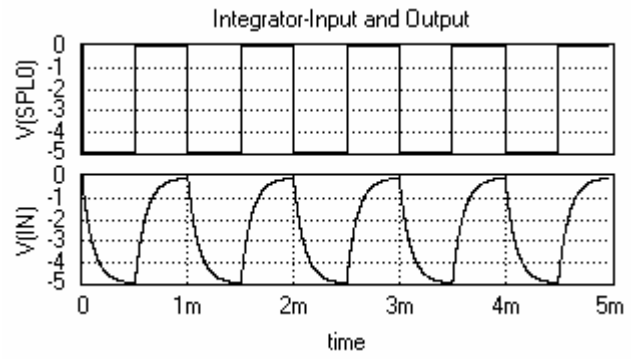


Fig 7.5

SPICE Control lines to obtain the output:

.PRINT: To display the result of each analysis in the textual format as a set of values.
Example:

```
Title: All_RC Coupled Amplifier:  - Noise Analysis
Date: Tue Nov 11 15:32:51  2003
Temperature: 27.000
Plotname: noise1:Noise Spectral Density Curves - (V^2 or A^2)/Hz
Flags: real
No. Variables: 3
No. Points: 601
Variables:
        0       frequency       frequency grid=3
        1       inoise_spectrumvoltage
        2       onoise_spectrum         voltage
Values:
 0      1.000000000000000e+001
        4.835175005850165e-012
        1.724455472037941e-016

 1      1.023292992280754e+001
        4.419038930816600e-012
        1.727586787447880e-016
```

. PLOT: To plot the points obtained after each analysis.
Example:

```
        Transient Analysis          Temp = 27.000 Deg C

Legend:  + = v(1)          * = v(2)
--------------------------------------------------------------------------------
time        v(1)   -5.00e+00-4.00e+00-3.00e+00-2.00e+00-1.00e+0000.00e+000
-----------------------|-------|-------|-------|-------|------
0.000e+000  0.000e+000 .       .       .       .       .       X
1.000e-004 -5.000e-002 .       .       .       .       .      X.
2.000e-004 -5.060e-002 .       .       .       .       .      X.
3.000e-004 -5.181e-002 .       .       .       .       .      X.
4.000e-004 -5.423e-002 .       .       .       .       .      X.
5.000e-004 -5.906e-002 .       .       .       .       .      X.
6.000e-004 -6.872e-002 .       .       .       .       .      X.
7.000e-004 -8.805e-002 .       .       .       .       .      X.
8.000e-004 -1.267e-001 .       .       .       .       .     +*.
9.000e-004 -2.040e-001 .       .       .       .       .     +*.
1.000e-003 -3.586e-001 .       .       .       .       .    + *.
1.100e-003 -6.679e-001 .       .       .       .      .+     *.
1.200e-003 -1.169e-000 .       .       .       .      +.     *.
1.300e-003 -1.883e+000 .       .       .      .+      .      * .
1.400e-003 -2.872e+000 .       .      .+      .      .*      .
1.500e-003 -4.190e+000 .      +.      .       .      *.      .
1.600e-003 -5.000e+000 +       .      .       .      *       .
1.700e-003 -5.000e+000 +       .      .       *      .       .
1.800e-003 -5.000e+000 +       .      .      *       .       .
1.900e-003 -5.000e+000 +       .      *       .      .       .
```

Types of Analysis supported by EDSpice Simulator

EDSpice provides different types of analyses as shown in Fig 7.6.

- ❑ Transient Analysis
- ❑ Small Signal AC Analysis
- ❑ DC Transfer Function Analysis
- ❑ Distortion Analysis
- ❑ Operating Point Analysis
- ❑ Noise Analysis
- ❑ DC/AC Sensitivity Analysis
- ❑ Transfer Function Analysis
- ❑ Pole-Zero Analysis

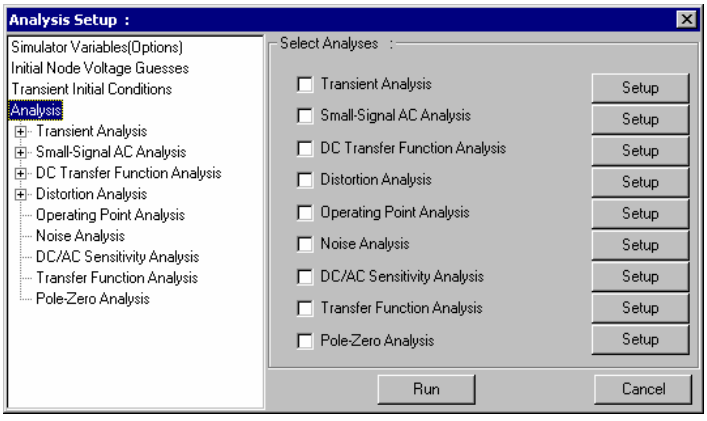


Fig 7-6

Transient Analysis

Refer sample project (EDWinXP/ Job/ MIXMODE_EDSPICE/ Amplif.EPB)

Procedure

Define parameters to the circuit elements-

Right click on the work space, select Change Simulation Parameter from Component Properties, then click on each component, and enter values except for those components having simulation references assigned to them.
Click on the AC source to pop up the Instance Parameter window (Refer Fig. 7-7) in which values are to be defined. Scroll down to get the instance parameter Source function. Click on the row corresponding to Source Function (last row of this dialog box) to get another window of Source function where you may select the source function and define the function parameters for the selected one. Select "Sine" from the list and specify the following parameter values.

Frequency 500Hz
Amplitude 1V

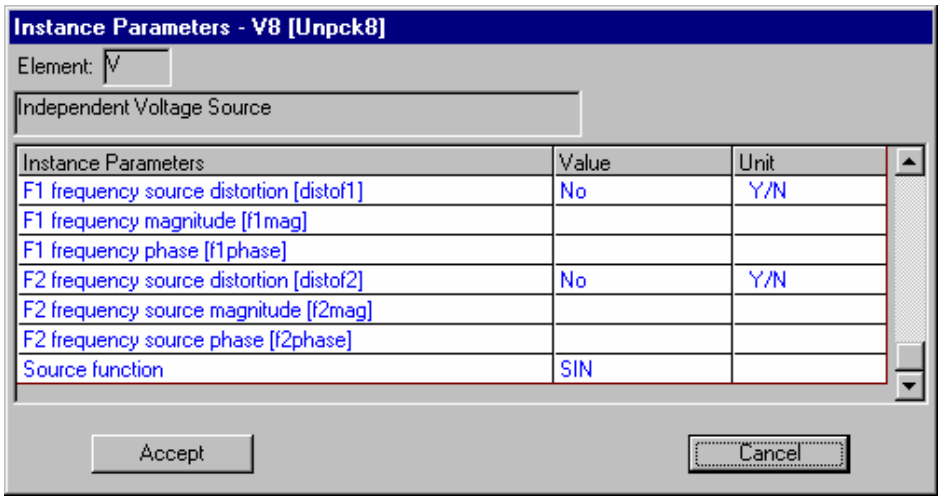


Fig. 7-7

Click ***ACCEPT*** to get the **Instance Parameter** window.
Similarly enter the simulation parameters for all the circuit elements.

Test the transient state of the circuit-

The transient analysis is done after setting the parameters for analysis. Select **Analysis/ Transient Analysis** from the tree view on the left side of the window and then give the necessary set up parameters in the Set Parameters on the right side of the window.

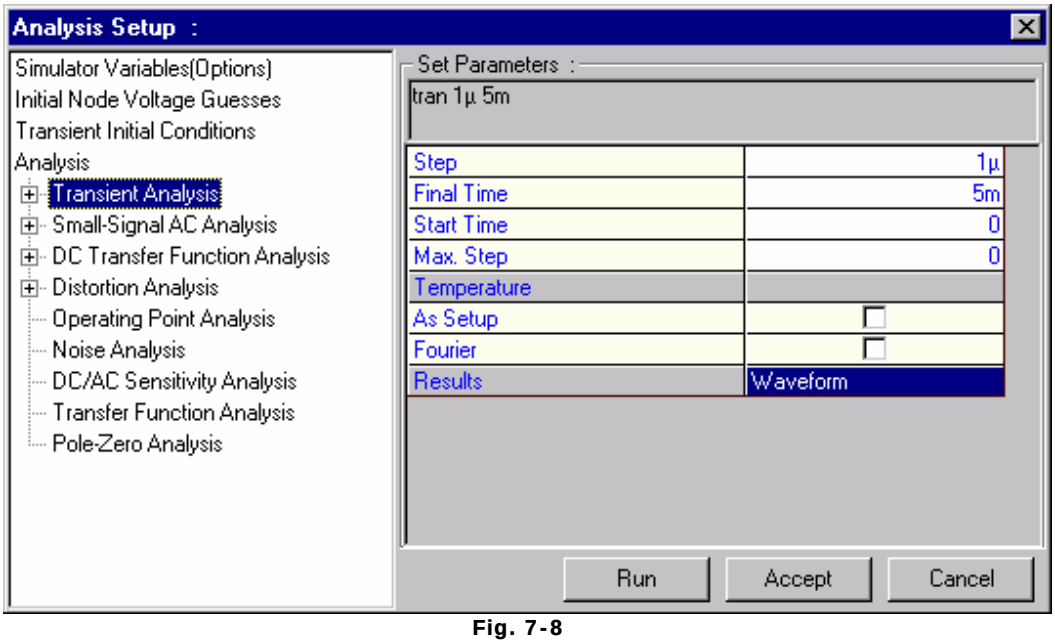


Fig. 7-8

Enter the required values for the parameters Step, Final Time, Start Time in the Analysis window. Indicate how the results are to be displayed (No Output/ waveform/ Standard Output) immediately at the end of the simulation. e.g.: Enter Step value as 1 µs, Final Time as 5ms and Start Time as 1µs.

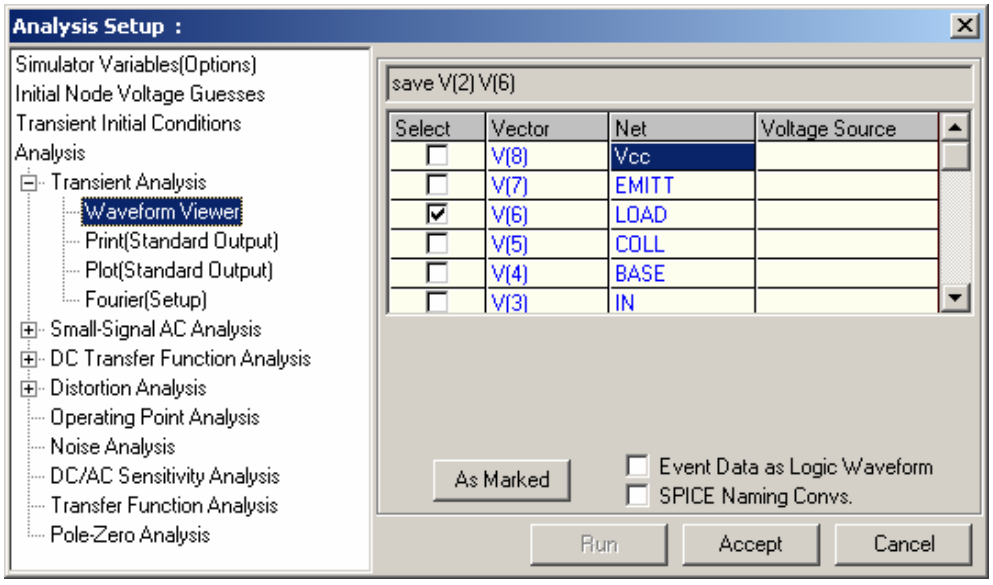


Fig.7.9

Click on Waveform Viewer option in the tree diagram under Transient Analysis to select the values to be displayed in waveform or click on As Marked button. (Fig 7.9) Click ***ACCEPT*** button to accept the changes and to automatically switch to ANALYSIS. Transient analysis is opted for analog circuits with inductors and capacitors. Click ***RUN*** button to start simulation

SPICE control line:

.TRAN TSTEP TSTOP	E.g. .TRAN 1µ 5m
.TSTEP – Step time	TSTOP – Final (stop) time

The simulation engine parses the netlist generated and when simulator engine has completed the analysis, the results of simulation are displayed in either graphical or textual form. The results are stored in the output files **RAWSPICE.RAW** and **EDSPICE.OUT**. The waveform viewer pops up with the result as shown below in Fig. 7.10.

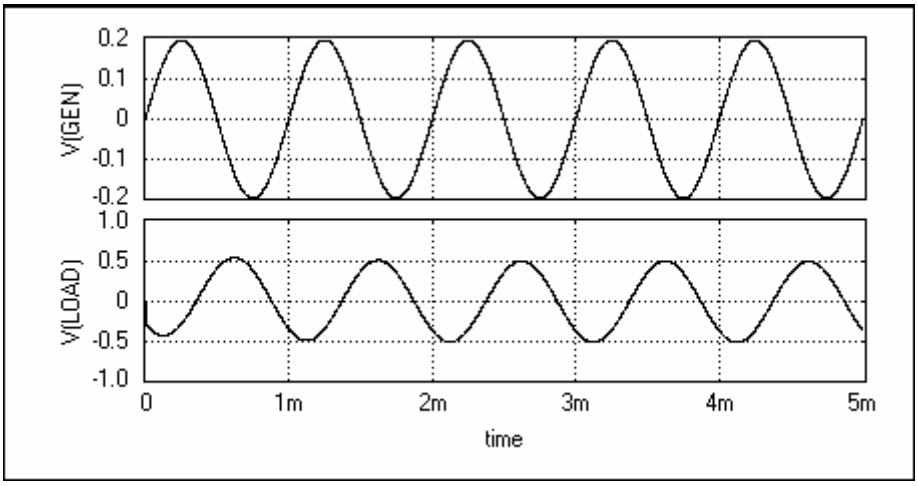


Fig. 7.10

Small Signal AC Analysis

Refer sample project (EDWinXP/ Job/ MIXMODE_EDSPICE/ Amplif.EPB)

Procedure

In order to run Small Signal AC Analysis, specify the analysis parameters by selecting Analysis/ Small Signal AC Analysis from the tree view. Specify the simulation parameters such as start frequency, end frequency, total points, Variation etc (Refer Fig. 7-11).

E.g.: For a given amplifier circuit, assign 10 as total points, Start Frequency as 10Hz and End Frequency as 1GHz and set the Variation as Decade.

If 'As Setup' is checked, the analysis is performed at a defined temperature. You can set temperature from the Setup menu / Temperatures. If this option is not checked, the operating temperature is taken as 27° C. Select the format by which results are to be obtained from Results dropdown and select from No Output/Waveform/Standard Output. Click on Waveform option in the tree diagram under Small Signal AC Analysis and either check the values whose waveforms are to be displayed or click on As Marked. Also specify the nature of the output waveforms-real/imaginary/magnitude/20 log10.

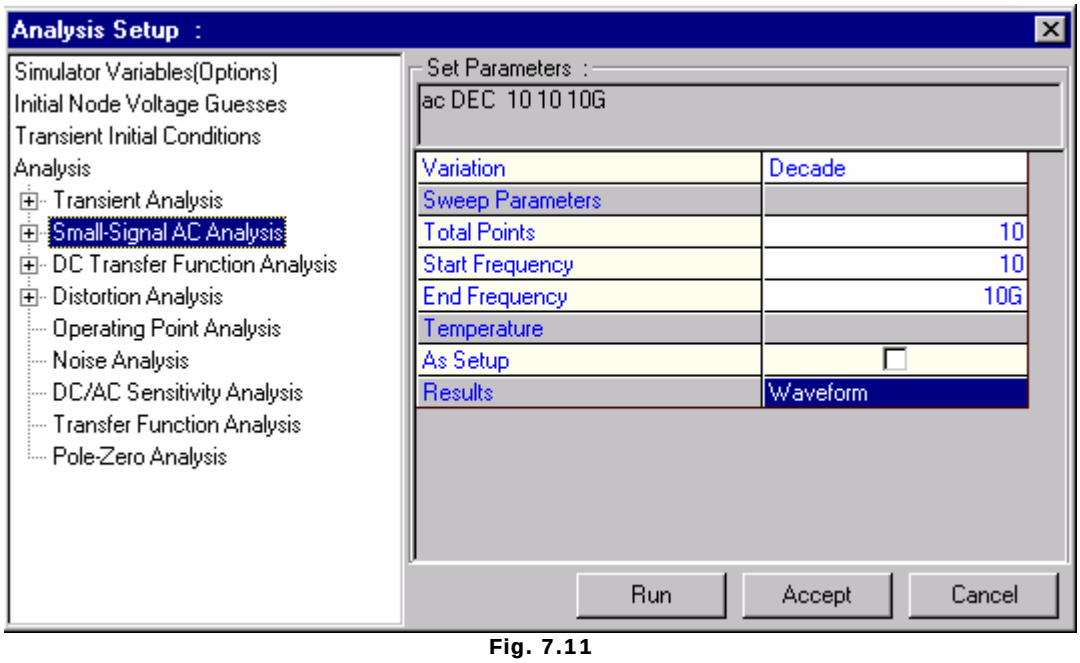


Fig. 7.11

Click ***ACCEPT*** button to accept these values and on RUN button to execute the analysis. In case you specified PRINT or PLOT results you may view it by selecting "Options -> View EDSpice Files -> Standard Output".

SPICE control line:

.AC LIN NP FSTART FSTOP	LIN NP- Linear no. of points
.AC DEC ND FSTART FSTOP	DEC ND-Decimal no. of frequencies/decade
.AC OCT NO FSTSRT FSTOP	OCT NO-Octal no. of frequencies per octave

FSTART-Start frequency **FSTOP-Stop frequency**

E.g.: .AC DEC 100 10 100K

DC Transfer Function Analysis

Refer sample project (EDWinXP/ Job/ MIXMODE_EDSPICE/ Amplif.EPB)

Procedure

In order to run **DC Transfer Function Analysis,** specify the analysis parameters by selecting **Analysis/ DC Transfer Function Analysis** from the tree view.

Since this analysis gives the behavior of the circuit with respect to varied voltage /current, two sources are required to run the analysis. Thus the variation of one value corresponding to changes in the other can be plotted. For this, specify the start and stop voltages for first and second source for which the analysis is to be done.

'Step' defines the number of points to be included for specifying the range of voltage on the X-Axis.

If 'As Setup' is checked, the analysis is performed at the temperature set from the menu Setup/ Temperatures. If this option is not checked, the operating temperature is taken as 27° C. Select the type of presenting results from 'Results' dropdown and set the parameters as per the selection made for Waveform Viewer, Print (Standard Output), Plot (Standard Output) and Fourier (Setup). Click **ACCEPT** button to accept these values and on RUN button to execute the analysis. In case you specified **PRINT** or **PLOT** results you may view it by selecting "Options -> View EDSpice Files -> Standard Output".

Distortion Analysis

Refer sample project (EDWinXP/ Job/ MIXMODE_EDSPICE/ Amplif.EPB)

Procedure

In order to run Distortion analysis, specify the analysis parameters by selecting **Analysis/ Distortion analysis** from the tree view. Specify the simulation parameters such as start frequency, end frequency, total points etc as shown in figure.

If you have two signals at the input, and you need a study of Intermodulation distortion, specify the value of F2OVERF1 and select the check box. If 'As Setup' is checked, the analysis is performed at the temperature set from the menu Setup/ Temperatures. If this option is not checked, the operating temperature is taken as 27° C. Select the result type from 'Results' dropdown and set the parameters as per the selection made for Waveform Viewer, Print (Standard Output), Plot (Standard Output) and Fourier (Setup). Click ***ACCEPT*** button to accept these values and on ***RUN*** button to execute the analysis. In case you specified **PRINT** or **PLOT** results you may view it by selecting "**Options -> View EDSpice Files -> Standard Output**".

SPICE control line:

.DISTO RLOAD INTER <…<…>>	RLOAD-Output Resistor
E.g.: .DISTO ROUT 5 0.5	INTER-Interval

This must be used along with .AC control line

Operating Point Analysis

Refer sample project (EDWinXP/ Job/ MIXMODE_EDSPICE/ Amplif.EPB)

The program should be informed about the results. The default selection is "As Marked". This means that results are displayed at all Voltage, Current and Logic State markers placed on the circuit. After analysis, the results will be presented by updating the markers. The values at all nodes and branches of the circuit, select "All Points". The results will be available in the default .raw file RAWSPICE.RAW located

at \.\EDS_WRK. You may view it by selecting "Options -> View EDSpice Files -> Rawfile"

SPICE control line:

.OP

Noise Analysis

Refer sample project (EDWinXP/ Job/ MIXMODE_EDSPICE/ Amplif.EPB)

SPICE is capable of modeling the following kinds of electronic noise:

- Thermal noise
- Shot noise and
- Flicker noise

Noise analysis is used to analyze the noise existing at any point in a circuit, due to the combined effect of all noise sources in the circuit.

Procedure

In order to run Noise analysis, specify the analysis parameters by selecting Analysis/ Noise analysis from the tree view. Specify the simulation parameters such as start frequency, end frequency, total points etc.

If 'As Setup' is checked, the analysis is performed at the temperature set from the menu Setup/ Temperatures. If this option is not checked, the operating temperature is taken as 27° C.

After analysis, the results will be presented as follows:

- the Noise Spectral Density curves will be presented in the Waveform Viewer.
- the total integrated Noise, (along with other data), will be presented in the .raw file RAWSPICE.RAW. You may view it by selecting "Options -> View EDSpice Files -> Rawfile".

SPICE control line:

- **.NOISE OUTPUTV INPUTSRC NUMSUM**
- **E.g.: .NOISE V(2) VIN 10**

- OUTPUTV-Output Voltage
- INPUTSRC-Input Source/Independent Voltage or Current source
- NUMSUM-Summary Interval

DC/AC Sensitivity Analysis

Refer sample project (EDWinXP/ Job/ MIXMODE_EDSPICE/ Amplif.EPB)

In order to run DC or Small-Signal AC Sensitivity Analysis, specify the analysis parameters by selecting Analysis/ DC or Small-Signal AC Sensitivity Analysis from the tree view. Specify the simulation parameters. If you require only a DC Sensitivity Analysis, make sure the "AC Sensitivity" check box is not selected. (However, make

sure it is checked if you want an AC Sensitivity Analysis.). If 'As Setup' is checked, the analysis is performed at the temperature set from the menu Setup/ Temperatures. If this option is not checked, the operating temperature is taken as 27° C. Select the type of presenting results from 'Results' dropdown and set the parameters as per the selection made for Waveform Viewer. Click ACCEPT button to accept these values and on RUN button to execute the analysis.

After analysis, the results will be presented as follows:

- the results of a DC Sensitivity Analysis will be presented in the .raw file RAWSPICE.RAW.
- the results of AC Sensitivity Analysis will be presented in the Waveform Viewer. The full results can be examined by selecting "Options -> View EDSpice Files -> Rawfile".

SPICE control line:

.SENS OV1 <OV2> OV1-Output Variable(Voltage or Current)

E.g:.SENS V(3) I(VIN)

Transfer Function Analysis

Refer sample project (EDWinXP/ Job/ MIXMODE_EDSPICE/ Amplif.EPB)

The magnitudes of the following quantities can be obtained by means of a Transfer Function Analysis:

- Voltage Gain
- Current Gain
- Transfer Impedance
- Transfer Admittance

In order to run Transfer Function Analysis, specify the analysis parameters by selecting **Analysis/ Transfer Function Analysis** from the tree view. Specify the simulation parameters (usually frequency and phase angle). Click ***ACCEPT*** button to accept these values and on ***RUN*** button to execute the analysis. After analysis, the results will be presented in the .raw file RAWSPICE.RAW.

SPICE control line:

.TF OUTPUTVAR INPUTSRC OUTPUTVAR-Output Variable(Voltage or Current)

INPUTSRC-Input Source(Small Signal Input Source, Voltage/Current)

E.g.: .TF V(10) VIN

Pole-Zero Analysis

Refer sample project (EDWinXP/ Job/ MIXMODE_EDSPICE/ Amplif.EPB)

In order to run Pole-Zero Analysis, specify the analysis parameters by selecting **Analysis/ Pole-Zero Analysis** from the tree view. Specify the simulation

parameters. Click ***ACCEPT*** button to accept these values and on ***RUN*** button to execute the analysis. After analysis, the results will be presented in the .raw file **RAWSPICE.RAW**.

SPICE control line:

.PZ NODE1 NODE2 NODE3 NODE4 CUR POL	**E.g.:**
.PZ NODE1 NODE2 NODE3 NODE4 CUR ZER	**.PZ 1 0 3 0 CUR POL**
.PZ NODE1 NODE2 NODE3 NODE4 CUR PZ	**.PZ 2 3 5 0 VOL ZER**
.PZ NODE1 NODE2 NODE3 NODE4 VOL POL	**.PZ 4 1 4 1 CUR PZ**
.PZ NODE1 NODE2 NODE3 NODE4 VOL ZER	PZ –Pole and Zero
.PZ NODE1 NODE2 NODE3 NODE4 VOL PZ	CUR-Current VOL-Voltage

Control line for Temperature:

.TEMP T1 <T2 <T3….>> **T1,T2 etc. are in centigrade.**

E.g.: .TEMP –30 150

SPICE Netlist Import

For details refer chapter- 2 - page: 77

Saving Circuit as a Subcircuit

If required the design may be saved as a subcircuit in the subcircuit library and later may be adapted to a symbol. The input and output nodes of the subcircuit must be assigned to appropriate entries of the symbol.

Assign subcircuit nodes

The dialog window Setup/ Subcircuit I/O Nodes allows to select subcircuit input and output nodes and arrange them in a proper sequence in the node list. Moreover, a short description may be attached to each node to explain its function. This description may be helpful for proper recognition of the nodes when a subcircuit is associated with a symbol.

Save as subcircuit

After assigning the subcircuit nodes this may be saved to the library by selecting "Options|Save as subcircuit".

Chapter 8

PCB Layout

Introduction to Layout Design

Layout Editor is used to design the PCB layout of a circuit. The project database supports design of 32-layers boards (28 electrical layers, 2 silk-screen & 2 masks). The design can be captured either in schematic capture or directly in layout editor. In the former case, the design is front annotated to the layout editor and in the latter case it is back annotated to schematic editor. When front annotated to the Layout, all packaged components on the schematic will be positioned in the layout at board datum (0, 0). PCB Layout can also be designed without a pre-existing schematic.

Components are automatically loaded as a result of packaging executed while editing the schematic diagram of the circuit. Layout may be started without schematic; In that case, new parts may be loaded on the board in similar fashion as in Schematic Editor. Location and orientation of components is defined either by manual relocation to desired position, using coordinates or with the help of auto placer. Traces may be routed manually with automatic via insertion whenever routing layer is changed. Sixteen types of user defined via pads are supported. Layout Editor also includes a number of online automatic functions to route/ reroute traces for single nets and to reroute existing traces for relocated components. Dedicated full board auto router and import /export interfaces are also integrated with PCB Layout Editor. Copper pour areas are defined as polygons and may be placed on any trace layer. Insertion of air gaps and thermal pads on artworks is automatic.

Design rules for manual, semi-automatic and automatic routing of traces and component placement are user defined and may be set individually for each project. Design rules violation, clearance errors and missing or incomplete connections are detected automatically.

The Design rules for the project may be set in the *Project Design Rules* window. This may be launched by *Project Explorer* | *Project* | *Project Design Rules (Refer page: 76).*

Configuring the Editor

Board Configuration

Default board formats for the workspace may be set in the *Project Explorer* | *System* | *Options window*. The user can select pre-defined formats or create own formats. It is advisable to set the required board size to avoid unnecessary wastage of space.

Features

- Maximum board size available - 4m x 4m.
- Maximum number of layers on board – 32 (28 trace layers, 2 silk screen & 2 masks)
- Available page formats – American & European.

American formats: AA , AB , AC , AD , AE , AF
European formats: EA , EB , EC, ED , EE , EF
By default American format AA is enabled.

Menu

Layer

Allows to select the layers on which the trace is to be routed the text is to be placed or Copper Pour Area is to be defined. The trace may be on any selected electrical layers. Each layer can be set to different colors in Project settings to differentiate between the layers.
E.g.: Default settings for Comp layer: Green color.

Tools
Displays a list of menu items that is present in Schematic, Layout and Fabrication Manager. The menu in this list differ in each editors and when selected allows entering into main object oriented function.

Tools(Components)
Enables component editing mode, presenting various tools that performs operation related to components.

Tools(Connections)
Enable connections editing mode, presenting various tools that performs operation related to connection between the components.

Tools(Texts)
Enable text editing mode presenting various tool that performs operations related to text

Tools(Block Edit)
Enables Block editing mode and presents various tools that performs operation related to objects like components/ wires in block.

Tools(Board Outline)
Enables Board outline editing mode presenting various tools required to perform operations related to editing the default board format.

Tools(Autoplace)
The tools required for autoplacing are displayed on the workspace when Tools| Autoplace menu is invoked.

Tools(3D Board Viewer)
Provides a 3D view of the entire board in X, Y or Z planes from different angles. It also provides the Controls to view the board from different directions. A 3D View Control dialog pops up, which assists in aligning the board in different angles.

Tools(Copper)
Edit Copper function enable to place conductive elements on trace layers. Conductive elements may be either of the graphic items (Copper planes) - Lines, Arcs, filled and unfilled Circles and Rectangles or a new type of item - Copper Pour Areas.

Copper planes are solid copper blocks where air gaps for pads/ traces may not be created. Such copper planes are usually used for shielding and as Keep Off Zones. It is recommended not to use these copper planes for distributing power supply or ground since Copper Pour Areas may be used for such purposes. In some cases, it may be necessary to relieve certain areas on the board from copper. This may be done by creating Copper Pour Areas in any shape. At least three vertices must be defined. This will relieve copper on the processed layer.

Tools(3D Trace Viewer)
Provides a detailed view of all the traces present on the loaded board by aligning the board in various angles. All the traces placed on the component layer may be viewed from top, while the solder layer traces may be viewed from bottom. Viewing the board from any other direction displays the traces present in other layers.

Tools(Via Padstack)
A dialog box Edit Via Padstack lists all the layers supported by the system. Selecting any layer highlights the other parameters associated with the padstack. The hole diameter may be specified in either inches or mm and the shape toggled between round and square. To make any changes to the default values, click on the necessary layer. The particular cell becomes editable. Enter the necessary values and click. To change the shape, click on the particular cell and select the shape. Click on ACCEPT to save the changes made.

Tools(Bury Vias)
Selecting this menu pops up a confirmation box to confirm burying the vias. On clicking YES, Buried Vias Layer Sandwich map dialog box opens. This dialog box provides information regarding vias present in the loaded database. Click ACCEPT button. The vias will appear only on the intermediate layers enclosed by the layers between which the electrical connectivity is made.

Tools(Unbury Vias)
When enabled, it simply unburies the vias. This implies that the vias will now be visible on all layers except on Comp. Print and Solder Print.

Tools(Characteristics Impedance Calculator)
Calculator is a tool to plan PCB stack up to achieve controlled impedance. It allows designing layer stack (from available EDWinXP layers), assigning layer type property (PWR/GND, Signals or Mixed) and other parameters (dielectric material, thickness of dielectric material, Cu thickness and trace width on signal layers).
Program automatically applies suitable characteristic impedance formula depending on layer configuration. (Microstrip, Stripline and Dual Stripline). It is also possible to

calculate required trace width, Cu thickness, thickness of dielectric, and permittivity for the layer when value of characteristic impedance is specified as a design rule.
A common dielectric materials Library is integrated with calculator. Entries in this library may be edited by the user and new materials added.

Preferences

Preferences (Active Layers on Top)
Allows displaying the active layer selected as the top layer, giving it priority over the other layers.

Preferences (User lay prefix)
Allows changing the component name prefix.

Preferences (Stacked Layers)
Allows displaying all the active layers stacked one above the other.

Preferences (Guidelines (Net))
Allows displaying a single ratsnest associated with the selected net while routing or relocating a trace

Preferences (Guidelines (Next Unconnected Node))
Allows displaying the next unconnected node of the net while routing or editing.

Preferences (Ratsnest for unconnected node only)
Allows toggling ON/OFF the display of ratsnest of unconnected nodes only.
Delete unnamed nets when connection is deleted
This option when enabled will delete nets that are not named if the trace is removed.

Preferences (T-connect Same Layer Only)
Allows T connections to be made possible only on the same selected layer while routing traces.

Preferences (T-connect Same Net Only)
Allows T connections to be made only on the same net while routing traces.

Preferences (Inherit Trace width from T Connection)
Inherits trace width from T Connection while routing new traces.

Preferences (Display Traces in XOR mode)
Toggles the display of traces in XOR mode.

Preferences (Reroute component connections after Move)
The option serves an important purpose of automatic reconnect the nodes of a component if the component is relocated or swapped.

Preferences (Auto Connect Settings and lists)
The execution of auto-connect functions may be controlled by setting different options in this dialog. It also contains lists of components currently scheduled for re-routing and list of currently routed lead-outs.

Preferences (Online Trace Clearance Check)
Displays if there is errors after routing the trace.

Preferences (Tear Drop pads)
Pops up a window Tear drop auto generation where the options (size and shape of the tear drop pads) for Tear drop generation maybe set.

Preferences (Auto taper after routing)
If tapered is set, any trace segment may be assigned different widths at the start and at the end. If the width at the end of a segment is smaller than at the beginning, then the segment will taper down gradually along its all length. In opposite case, such a segment will taper up from smaller to bigger width. This function also creates smooth change of width in cases when thicker trace must be routed between pads.

Preferences (X /Y/Z Coords)
Allows determining the current cursor position with respect to a given reference point in terms of the X, Y and Z coordinates. The values are displayed in the position toolbar.

Preferences (Center)
Allows setting the origin coordinates to the Center. The co-ordinate information displayed in the position toolbar is with reference to a point on the board. This defines the center of the board as reference point for all coordinate and dimension information.

Preferences (Board Datum)
Allows setting the origin coordinates to bottom left corner of the board.

Preferences (Refpoint)
Allows setting the position of the origin coordinates on the workspace with respect to a reference.

Preferences (Lock Toolbar)
Anchors all the toolbars at the placed location.

Preferences (Meshed Copper Pour Areas display)
Enables to view the meshed copper pour areas present in the layout.

Auto
This drop down menu allows performing automatic function such as placement, fanout and renumbering of the components in the circuit, routing of traces etc in the most optimum manner. It also allows setting layers for the clearance check.

Auto(Autocheck)

Clearance Check Setup dialog box allows to set up clearance parameter value, **Other DR Violations** tab in this window is used to set other clearance check parameters and **Global test report** tab allows to execute all available tests in proper order and produces test report containing details of all detected problems.
The Parameters include

- Pad to Pad distance
- Pad to Trace distance
- Trace to Trace distance
- Channel width for single trace check

Also allows toggling ON/OFF the layers on which the check is to be performed. After proper setup of the values, the system is ready to perform Auto check on the board.

Auto(Autorouter)
Allows routing the current Project automatically by selecting any one of the three autorouters available. The three menu items listed under this are:

- Autorouter - Arizona
- Autorouter - Specctra
- Autorouter - Maxroute

Arizona Autorouter

Arizona auto router is an integrated module of the EDWinXP. It uses its own temporary project and simplified graphics. The Arizona auto router allows routing the traces of a PCB Layout automatically. The netlists is given as the input to the auto router. When this router option is selected, all non orthogonal traces will be removed and accepts only orthogonal traces as prerouted traces.
Various options such as load Pre routed traces (only orthogonal traces); load copper setting layers etc may be set before autorouting. With these options set, system initiates the routing process. The original project is visible in Layout editor until you update the main project from the autorouter.

SPECCTRA Autorouter

SPECCTRA auto router is an integrated module of the EDWinXP and is designed to handle high density printed circuit boards that require complex design rules. SPECCTRA autorouter uses powerful Shape Based algorithms to make the most efficient use of the PCB routing area. The results are high completion rates while following high speed electrical rules.
SPECCTRA conserves system resources by not using memory consuming grids. It handles staggered pin components and routes through them with ease. Its diagonal routing algorithms, operating in either grid or grid less mode, handle components of non-standard dimensions that previously required manual routing.

MaxRoute Translator

The MaxRoute Translator is an application that allows converting layout project (database) to a form that is acceptable to MaxRoute Autorouter and MaxRoute Autoplacer. It outputs all the information necessary to reconstruct the system layout project (database) in MASSTECK. This module may also be used to import routed traces from MaxRoute Autorouter as well as results of MaxEDS Autoplacer.

Auto(Autofanouts)
Provides option to setup selected net fanout parameters and generate fanout on the board. SMD pads may be connected to copper pour areas (ground or power supply) in following manner:

1. Copper pour on Component or Solder side layers if the component is placed on this side of the board.
    a. Pads may be soldered directly to copper.
    b. Pads may have heat relieve items in the pad stacks, which must be shaped in such way that they provide proper through pass from copper to pad
    c. Pads may have a trace stub with air gap = 0, which will provide conductive bridge over pad's own air gap to surrounding copper. This type of connection is called fanout without via hole.
2. Copper pour on middle layers.
3. Pads are connected to copper by short trace stubs terminated by via hole. Via holes provide necessary connection to copper underneath. This type of connection is called fan out with via hole.

Auto(Autorenumber)

When a schematic is converted to a layout, the placement is governed by shortest length of connectivity, ease of routing, functional organization etc. After completing the layout, it is necessary to order the components to aid manufacturing stage at the assembly shop and to help ease of testing.
Autorenumber allows re sequencing the components on the layout in a specific order by setting the given parameters in the dialog box. Component prefix and starting number may be entered with respect to certain parameters such as board corner, coordinates, directions etc. Channel width may also be specified. Click ***ACCEPT*** once the selection is complete.
If the component prefix given in the dialog box is not matching with any of the components in the loaded database the system issues an appropriate error message.

Auto(Net Trace Integrity)
Ensures that project integrity has not been corrupted. In rare cases the internal cross references between objects in the project (database) may get corrupted. It may cause malfunctions of the system. This function performs test of internal cross-references. If some references point to missing objects then the referencing object is deleted from the project (database). In most cases objects containing references to missing object cannot be deleted any other way because they are invisible on the screen. It is useful to execute this function from time to time to ensure that project (database) integrity has not been corrupted.

Info

Info(General)
Opens a dialog box where information regarding the objects placed in the workspace may be obtained.

Info(Statistics)
Pops up a PCB Layout property window that displays all information related to the board such as board dimension, number of components, pads, holes for pins, via holes and total holes etc.
This also gives information about the layer usage such as layer name, number of trace segments, pad items and copper items in each layer.

Info(Buried Vias)
Opens Buried Vias Layer Sandwich map dialog box that allows display of information on the buried vias used in the loaded project. If no buried vias exist, a message box displays buried vias not found. If there are any buried vias in the layout, the layers sandwich Info is displayed, which shows the number of buried vias and the layers on which they are created. A cross mark placed against a layer indicates that a buried via exists in that layer.

Info(Density Graph [Theoretical])
Opens Connections Density Graph (Theoretical) dialog box that is used to obtain a theoretical view of trace density defined on the board. The setting panel of the Density graph consists of various options, which may changed accordingly.

Info(Density Graph [Actual])
Opens Connections Density Graph (Actual) dialog box that is used to obtain an actual view of trace density defined on the board. The settings panel of the Density graph consists of various options, which may changed accordingly.

Info(Errors)
All the clearance error statistics can be viewed using the Errors option. All the layers will be listed in the window that pops up. The system recognizes six different types of errors. These are:

#1 Pad too close
#2 Pads on Pad
#3 Pad / Trace / Items too close
#4 Pads on Trace / Item
#5 Trace / Items too close
#6 Trace / Items X-ing
#7 Shortcuts to copper pour
#8 Non orthogonal traces

For each layer the number of errors is displayed in respective columns. The total number of errors is displayed in the Total column.

Steps to follow to define board outline

i. Select  **Board Format** from Tools toolbar.
ii. Select the function tool  **Define Outline**.
iii. The option tool  **Create Board** will be enabled. This tool enables free hand drawing, using which a board of desired shape can be drawn on the workspace.

iv. To select a pre-defined board format, select the option tool **Textual Mode**. The Properties Board Outline (Create) dialog pops up as shown in Fig.8.1.
v. Enter the desired values and click ***ACCEPT*** button.

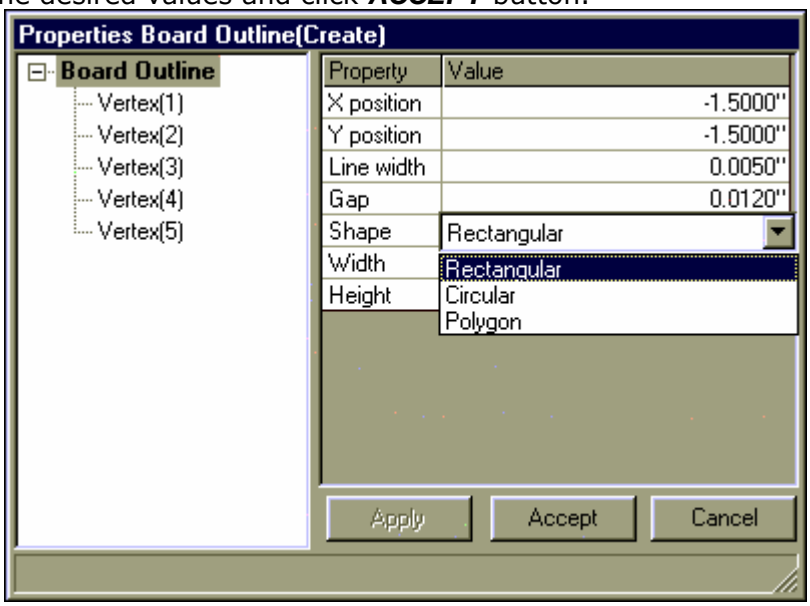


Fig.8.1

Starting of Layout Editor:

This module may be invoked from Project Explorer in the following ways.

- Right click PCB Layout and select Edit PCB Layout from the list or Double click PCB layout
- Select Edit PCB Layout from the task list or from the task toolbar.

Loading components

This section deals with how to extract components from the respective libraries and position them on the layout editor. The components placed on the schematic, which contain both symbol and package, are front annotated to the layout after packing. These components are positioned at board datum (0, 0) automatically and can be relocated either manually or automatically. If new parts are required to be added, they may be extracted as part using options of the function tool **Open part library**.

Only parts that contain both symbol and package will be automatically back annotated to the schematic.

Components can be loaded in the working area using any one of the following three ways:

i. Component Browser
ii. Using Library Explorer

iii. Using Library Browser
iv. Add Components

Select **Open part library** function tool to display the last three option tools.

Placing the Component in Layout

This section deals with the layout creation of Half Adder. All the components for the Half Adder is already packed from the schematic (refer page 142), so they are automatically front annotated to the layout and will be positioned one above the other at the board datum. The netlists information will also be updated simultaneously, which make the routing easier.
Before we start loading Parts on to the page, turn ON Grid by enabling grid from the dropdown, in Standard Toolbar. The value for grid may be selected from the drop down list as .1000". Similarly, set Snap value to .0500" for better placement of the components.

Select Components from toolbar and right click on the workspace to popup a set of Component editing tools. By default this tool is invoked with the Relocate Component tool enabled.

Keep a margin of 400mil from boundary of the board.

The components may now be relocated in the following way.

1. Click on the component .A confirmation box pops up to show the selected component. Select ***YES*** if the selected component is U1 or else select NO till U1 is selected. Move cursor to a position well within the board to place U1. To orient this component by 90° / 180° / 270° on the board, click **Rotate Component by 90 degree** tool or press F1 key to rotate the component until it is in the required position. Press F1 3 times to place the component as shown below. Click mouse to place the component. Select the function tool **Relocate the Component by name** and place it below the component.

Tips: Enable **Ratsnet** option tool of **Relocate Component** function tool to view ratsnest while relocating the components to ensure that components having a large number of interconnections are positioned close to each other. Pressing SHIFT key while relocating/ stretching an item allows the item to move/ stretch smoothly.

2. When a component is being relocated, all other component placed at board datum will disappear which reappears on **Redraw**.
3. Place U2 and J1 in the same method described above. Final placement should appear as shown in Fig.8.2.

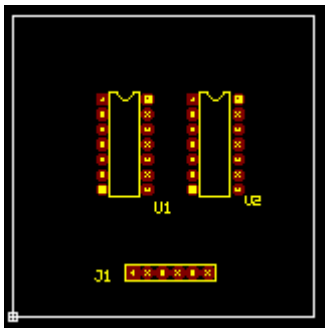


Fig.8.2

Next topic guides you through routing the PCB board.

Routing the Board

Connections between components may be established by using **TRACES** and **COPPER POUR** areas. Click **Route** from Tools toolbar to enable a set of Routing tools on right clicking the workspace.

Tips:
Adjust zoom precision to view the pins properly.

Turn on Preference/ Guidelines (Next unconnected node) before routing because this option guides you to take the easiest path to route.

Select True Size and Pad frames from View/ Layout, enabling you to select proper trace size. This also prevents you from creating errors such as traces crossing over pad, traces very close together etc.

First route power and ground signals (Net SPL0 and +5V). In Project Explorer, select Project / Project Design Rules and set the routing width to 0.030" for Pwr/Gnd lines and 0.013" for Signal lines.
To start routing traces, first select the power points; say pin 14 of U1 and route to pin 14 of U2.

The steps to complete this connection are as follows.

The trace connection may now be created in the following way.

1. Right click and enable tool **Route** to start routing connections. Select layer for routing from **Layers** in the main menu. 28 layers are available for routing. By default **COMP LAYER** is selected. Click on pin 14 of U2 to route on **SOLD LAYER**. A small triangle appears at this pin and cursor changes to a crosshair with a square. The next node in that net is displayed with ratsnest ending with a rectangle as shown in Fig.8.3.

Tips: While routing, enable the tool Snap Trace by 45 degree to change routing directions in steps of 45 deg only.

To route curved traces, select the option tool  *Toggle arc insert (F11) to change routing directions in arcs.*

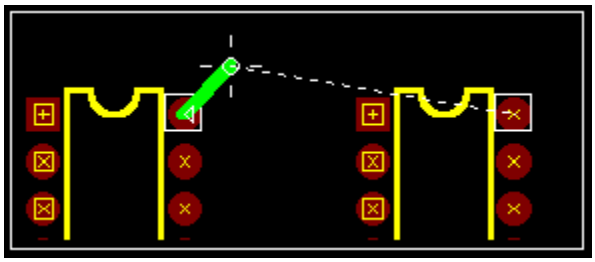


Fig.8.3

2. Move cursor with 45° angle through a short distance and click at the nearest point as shown below. The first segment has now been anchored. Now take this trace horizontally and click near 14th pin of U1. Once again take bend point at 45° angle and connect the trace to 14th pin of U1.

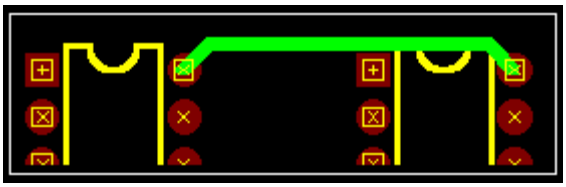


Fig.8.4

3. Terminate routing of the trace by pressing END or F4 key on your keyboard. Or click on the tool  **End Connections**.

4. Connections of 5V net have been accomplished by traces. The Ground net connections can be done by using a copper pour area. Select  **Copper** from the Tools toolbar. Select the second Function tool  **Create Copper graphic item** and select the fifth option tool  **Create copper pour area**. Now select the net to which the copper pour should belong by selecting SPL0 from the dropdown list box 

in the Sizes toolbar. Now start creating the copper pour polygon by clicking near the 7th pin of U1. Clicking on any point introduces a vertex at that point. Enclose the 7th pin of U2 and the entire connector, then right click and press 

Finish Copper Pour Create.

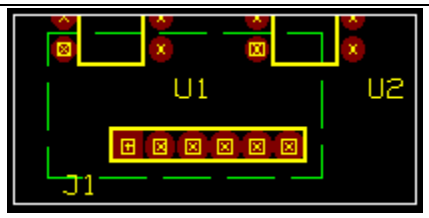


Fig.8.5

5. Semi-autorouting functions can also be used to route connections. Select the function tool **Auto Connect Traces**. Select the first option tool **Auto Connect Node Pair** and click on the 2nd pin of U1. A rubber band like connection shows where it has to be connected as shown in Fig.8.6.

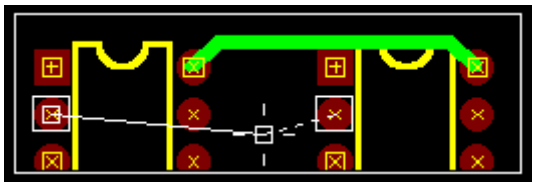


Fig.8.6

Click on the node where the rubber band connection ends, i.e. pin2 of U2 and the connection is automatically routed, now press **End Connection**.

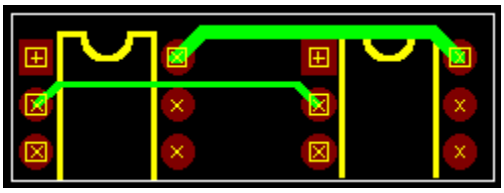


Fig.8.7

6. Uses the second option tool Auto Connect net to autoroute a net. Click anywhere on the workspace, an input box appears, enter the name of the net, which has to be routed, say A. Clicking on a node belonging to the net A will also achieve the same result (i.e. clicking on pin 1 of U1).
7. Repeat the same procedure as in (5) for the nodes at pin 3 of U1 and U2 respectively as well as the rest of the unconnected nodes on the connector.

Use Layout Editor / Auto / Autorouters / Arizona to autoroute the board.

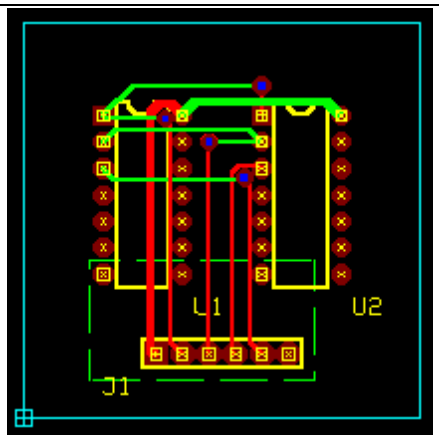


Fig.8.8

To avoid errors

1. While routing, click on pins and then enable the tool  Pin to pin. This will allow routing between pins and ensures proper connection.
2. Routing between pads should be done carefully, else trace connections get merged to the pads thus producing errors. This may be avoided by enabling True size ON from View menu, thus while routing the board; trace-pad distance may be noted and changed.

Assign Nets

Entry points having electrical connections in schematic are highlighted as nodes in the layout. Net is a collection of nodes that are electrically connected together. The creation of a trace automatically results in creation of the corresponding Net. A trace is merely a visual representation of the corresponding net description.

Deletion of a trace removes only the trace but does not remove the Net whereas deletion of a net removes ALL associated traces. The deletion of a node in the net removes corresponding connection in the net and removes associated TRACE SEGMENTS also.

Creating Nets

User can create a Net connecting the desired entry points using the available tools. The system by default assigns name to each net (E.g. UN1, UN2 etc. - UN stands for UNNAMED) and these may be edited or renamed according to user's convenience.

Net Names

The default net names (UN1, UN2 etc…) assigned by the system may be renamed according to the function it performs. System allows naming the net as PWR/GND, NAMED (RESET, CLOCK…) and UNNAMED nets (UN1, UN2....).

Advantages of using Net names:

i. Editing the nets in complex project becomes simpler.

ii. Net names indicating the function makes job easier in identifying the nets and is helpful while simulating the circuit.

iii. The other advantage of NAMED nets is that while working with complex circuit, a different designer would come to know the status of the net to be NAMED net, so that this information prevents that user from tampering the net name.

Default Nets

The power and ground pins are assigned to the part at the time of part creation. These are referred as SPL1 and SPL0 respectively and are called the Default Nets. After packing components in the schematic, these nets are automatically represented as nodes in the layout.

Select Info/ General/Nets in Layout Editor to view all the Nets that are already assigned. By default SPL0 and SPL1 will be listed.

Net Priority

Priority is first given to PWR/ GND, then NAMED nets and then to UNNAMED nets. While merging, when a NAMED net is merged to UNNAMED net, the resulting net has the name of the NAMED net. In the same way, when a PWR/ GND net is merged to NAMED net, the resulting net has the name of the PWR/ GND net.

Incase of nets having the same priority, the second net selected gets merged into the first net; i.e. if two UNNAMED nets UN1 and UN2 are to be merged, and if UN1 is first selected and then UN2, the resulting net has the name UN1.

Autoroute Traces

A set of tools has been provided to automatically route the traces between selected nodes and selected net. Autorouting can be done by either using the function tool Autoconnect Traces or by using any one of the three available autorouters.

How to route using the function tool?

i. Select the function tool **Autoconnect traces**.
ii. To autoconnect selected nodes of a net, select the option tool Auto Connect Node Pair. Click on any node of a net. The trace gets connected to the node and remains tagged to the cursor showing a connection to the next nearest node of the selected net. Move the mouse to the next node and continue this process till the last node of the selected net is connected. END key completes the current routing action. This is a semi automatic process.
iii. To connect a selected net, select the option tool Auto Connect Net. Click on any node of a net. A confirmation box pops up confirming the route. Click Yes to route the trace. All nodes of the selected net get routed.

If the menu Preference/ Miter Autorouted connections is enabled while using these Auto Connect tools, all trace connections are mitered i.e. the traces get a 45° bend.

☛How to use Arizona Autorouter?

Select **Auto➔Autorouters ➔Arizona** from the Layout editor menu bar.

The function toolbar of Arizona autorouter is explained below:

Parameters setup

Routing Parameter Setup
This option pops up Routing Parameter Setup to set routing directions for the selected layer, set clearances between pads, vias and traces, setup routing scheme and wrong layer cost for the design, to set trace width & to select via padstack for Pwr/ signal connections, set fanout routing parameters, setting optimize costs parameters such as Trace right direction, Trace wrong direction and Vias. Toggle ON/OFF routing of Pwr and/or signal connections. If the settings in Default Design Rule dialog is to be used, then enable the options provided.

Routing net parameters
This option pops up Net Parameters to set routing parameters for individual nets & net groups. Click on each net to pop up Design Rule set dialog where the necessary options may be set.

Interactive routing

Selected pad pair
Option to route traces for selected pad pair.

Delete & reroute selected trace
This option tool allows deleting a single trace and rerouting it again.

Selected component
This option tool allows to route all traces connecting selected component.
Delete traces of selected component
Option to delete all traces connecting selected component. With this tool selected, click on the component whose trace connections are to be removed. All the routed traces of that particular component get deleted immediately.

Fanouts for selected component
Option to preroute fanouts for selected component. Select this tool and click on the component whose fanouts are to be prerouted. The escape wires for the components gets prerouted.

Fanouts for selected net
Option to preroute fanouts for selected net. Select this tool and click on any of the nodes of the net whose fanouts are to be prerouted. The escape wires for all the pads in the net gets prerouted.

Fanouts for selected SMD pad
Option to preroute fanouts for selected SMD pad. Select this tool and click on the SMD pad whose fanouts are to be prerouted. The escape wires for the selected pad gets prerouted.

Auto routing routines

Fanouts on whole board
This option tool allows to preroute fanouts for whole board. When this tool is selected, the escape wires for all the components (for the entire board) gets prerouted.

Start autorouter
Option to start router in full auto mode. This option tool when selected starts the execution of the autorouter. Routing is done according to the settings made. The status bar shows the percentage of completion of the routing.

Remove redundant vias
Option to remove redundant vias. On selecting this tool, the redundant vias are removed and the whole trace gets re-routed in a single layer.

Clean up
Option to clean up the design after routing. After routing, selecting this option tool optimizes the layout project by deleting the unnecessary trace loops or trace segments, which have been created.

Test for conflicts
Option to remove clearance and route rules conflicts. Select this tool after routing. The number of traces tested and number of traces found OK. Are shown in the status bar at the bottom. In case any contrariety is found with the traces, they are removed. The traces thus removed can be identified using the tool Display list of unrouted pairs. The routing may be done anew to get rid of the contrarieties.

Optimize
Option to optimize routed results taking into consideration, the optimization cost parameters and the weight of the traces, which result. During optimization the router tries to reroute every trace and if it gets weight of new trace less than previously routed then it deletes old trace and puts new one to the project, otherwise nothing to be done.
To remove as much vias as possible 'Via Cost' should be setup as at least 1000.

List of unrouted pairs

This option tool displays the list of unrouted pairs in the design. This option tool when selected pops up a dialog box listing the unrouted pairs. The copy screen to clipboard button may be used to copy the list of unrouted pairs in case it is required for say, verification purposes.

Miter
Option to miter all orthogonal traces & finish autorouting. When this tool is selected, a dialog box pops up to confirm the mitering operation because once it is executed; re-entry to the autorouter is not allowed.

☛How to use SPECCTRA Translator?

From the Layout Editor, select the menu Auto | Autorouter | Specctra.
The Specctra Translator window is as in Fig 8.9

Fig.8.9

Translate project to SPECCTRA design file
Using this option the currently loaded project (database) can be converted to be compatible with SPECCTRA design file format. Before translating the project (database), the parameters for trace widths, vias and grids, the clearances and the trace type to be routed on the layers etc. are to be set. This can be done using setup from the menu bar.

Import results from SPECCTRA Autorouter
Using this option the SPECCTRA Autorouter results stored as SPECCTRA Routes files (with extension .rte) may be imported to the current project (database). The traces in the current project (database) will be replaced by the imported results. On clicking EXECUTE, a confirmation box pops up to confirm that the traces may be replaced.

Import results from SPECCTRA Autoplacer
Using this option the SPECCTRA autoplacer results stored as SPECCTRA Place files (with extension .plc) may be imported to the current project (database). On clicking EXECUTE, a dialog box pops up to select the required Place file. The components will be relocated as per the positions specified by the imported file.

☛How to use MaxRoute Translator?

From the Layout Editor, select the menu Auto | Autoroute | Maxroute.

The Maxroute Translator window is as shown in Fig.8.10.

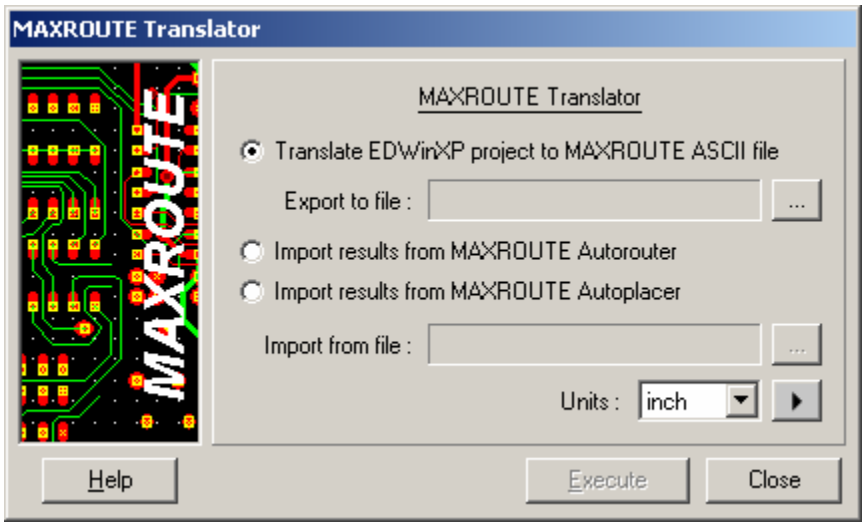


Fig.8.10

Translate Project to Maxroute ASCII File
This option allows to translate the currently loaded project (database) to MASSTECK ASCII file (files with .MIN extension) that are acceptable to Maxroute Autorouter and Maxroute Autoplacer. This file includes pad code assignments, packages, copper areas and layout texts, which will be treated as keep-out areas.

Import Results from Maxroute Autorouter
This option allows importing the results of Maxroute Autorouter back to the system. All traces in the current project (database) will be replaced by imported results (routed traces) from Maxroute Autorouter, which are stored as MASSTECK ASCII files with the .MIN extension. The file to be imported should correspond with the currently loaded project (database).

Import Results from MaxRoute Autoplacer
This option allows importing the results of MaxRoute Autoplacer back to the system. All components in the current project (database) will be relocated according to imported results from MaxEDS placer and stored as MASSTECK ASCII files with .MIN extension. The file to be imported should correspond with the currently loaded project (database).
Operations that may be performed on a trace after routing

Refer chapter 4

☛How to select connection(s)/ nets(s) by marking with bullets?

Refer Chapter 4

Properties of a trace

☛How to invoke property window and edit properties of trace?

Select (bullet) the object (trace) first and right click on the trace. In the pop up menu, choose Properties/Trace to display the property window as shown in Fig.8.2

Net Displays the net name.
Width The width of the trace segment may be changed here.

Gap The airgap size may be set using this field.
Layer Allows to select the placement layer for the text

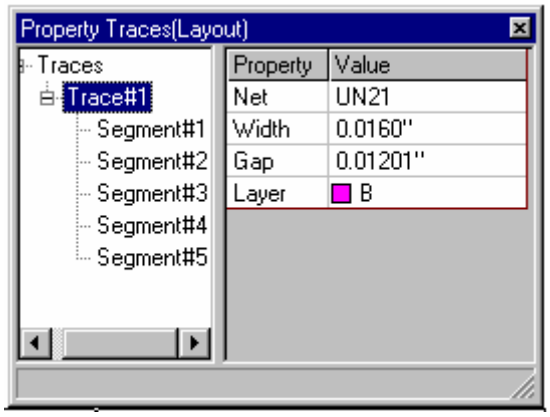


Fig 8.11

Property window is also invoked when you double click on the object (components, traces, text copper pour item etc.) provided the selected tool on the toolbar does not perform any function.

The common parameter changes related to different traces (when more than one traces are bulleted) such as trace width, airgap and layer name may be changed from this panel. To do so, click on Traces in the left windowpane to display these parameters. Against these parameters, change the sizes/ select the layer. The individual trace and segment parameters may be viewed/ changed by clicking on the respective trace/segment found on the right pane in this property window. The segment parameters include width, airgap and placement layer, which may be changed or its position and length of the segment may be viewed.

How to invoke property window and edit properties of net?

Select (bullet) the object (net) first and right click on the trace. In the pop up menu, choose Properties/ Net to display the property window as shown in Fig.8.12.

Name Displays the net name that is mandatory.
Status The status of the net may be set to either Power/ ground, Named & Unnamed.
Trace width The width of the trace segment may be changed here.
Air gap The airgap size may be set using this field.
Layer Name The placement layer of the trace segment may be selected.

Property window is also invoked when you double click on the object (components,

traces, text copper pour item etc.) provided the selected tool on the toolbar does not perform any function.

The common parameter changes related to different nets (when more than one traces are bulleted) such as status, trace width, airgap and layer name may be changed from this panel. To do so, click on Nets in the left windowpane to display these parameters. Against these parameters, change the sizes/ select the layer. The details regarding the pins of the same net are displayed by selecting each pin under each net name. The parameters that may be viewed are Layout component name, Pin number, Connected or not, Schematic component name, Schematic entry number, found in schematic page.

Testing the Board

While designing a PCB, it is obvious that a number of errors may occur. These errors may be in the form of overlapping pads, unconnected NODES, traces crossing another trace, etc. Such errors must be taken care of before printing the PCB. To find out such errors, certain checks on the board. Connectivity and DRC check are two methods by which the errors may be generated on the board and using the necessary tools, these errors may be rectified.

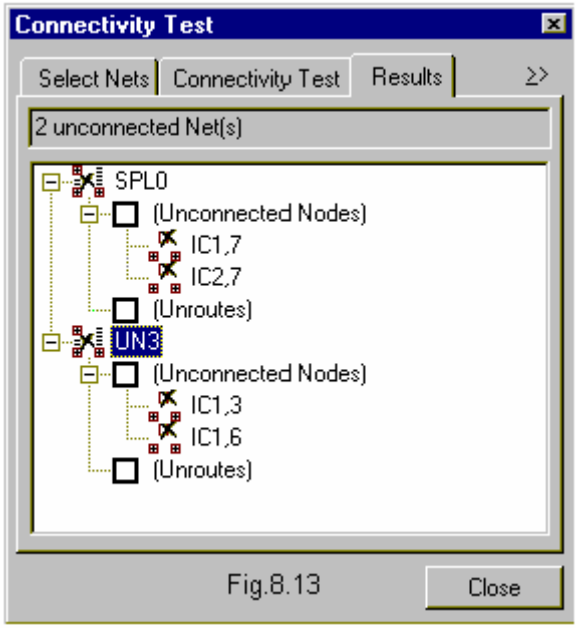


Fig 8.12

Connectivity Test

Connectivity test may be used to check whether there is any electrical discontinuity (unconnected nodes or deleted trace segments) in a single net. By setting certain parameters, the test can be performed either on individual nets or all the selected nets. It can also be specified whether to stop the test and display the results when the first discontinuity is encountered or to continue the test for all nets even if discontinuities are encountered and display the entire results at the end.

☛How to perform Connectivity Test?

i. Select  **Connections** from Tools toolbar.

ii. Select the function tool  **Connection Property**, select the option tool  **Test Connectivity** and click on the board or on a net. The Connectivity Test dialog pops up.

iii. Select the required nets using the move keys and click the **connectivity test** tab.

iv. Under Connectivity test tab, set anyone of the three options:
- **Stop at first fail:** Test stops at the first occurrence of error.
- **Test all selected Nets:** Checks whether all NODES of the selected NETS are connected.
- **Test single Net:** Checks connectivity of the NODES of the selected NET.
- Click the ***TEST*** button to display the results.

v. Perform this test until "Tested Nets – Fully Connected" message is displayed in this window.

Design Rule Check (DRC)

This utility is used to create an error free board to enhance the efficiency of your board. It automatically smoothes, miters, and checks for both aesthetic and manufacturing problems that might have been created in the process of manual or automatic routing. Number of design violation parameters may be used to verify the layout of a board. Layout conducts a design rule check with the parameters checked and any problems are marked by an Error label and may be queried using the Redraw/ Error. The design rule settings may be saved as a permanent setting or may be set for the circuit or for the current project only.
This test helps us to check the clearance between pad to pad, pad to trace and trace to trace.

☛How to perform Design Rule Check?

1. Select **Autocheck** from **Auto** Menu. The **Auto Check Setup** dialog pops up as shown in Fig.8.14.
2. Select the layers and enter the clearance value in the window. To select all the layers used in the project click the ***SET TO USED*** button.
3. If any Design parameters are used for the project then check Use Clearances as in Design Rules. Click on **Check other DR Violations** tab and set the required options. For more information on this please refer main help.
4. Click ***EXECUTE***.

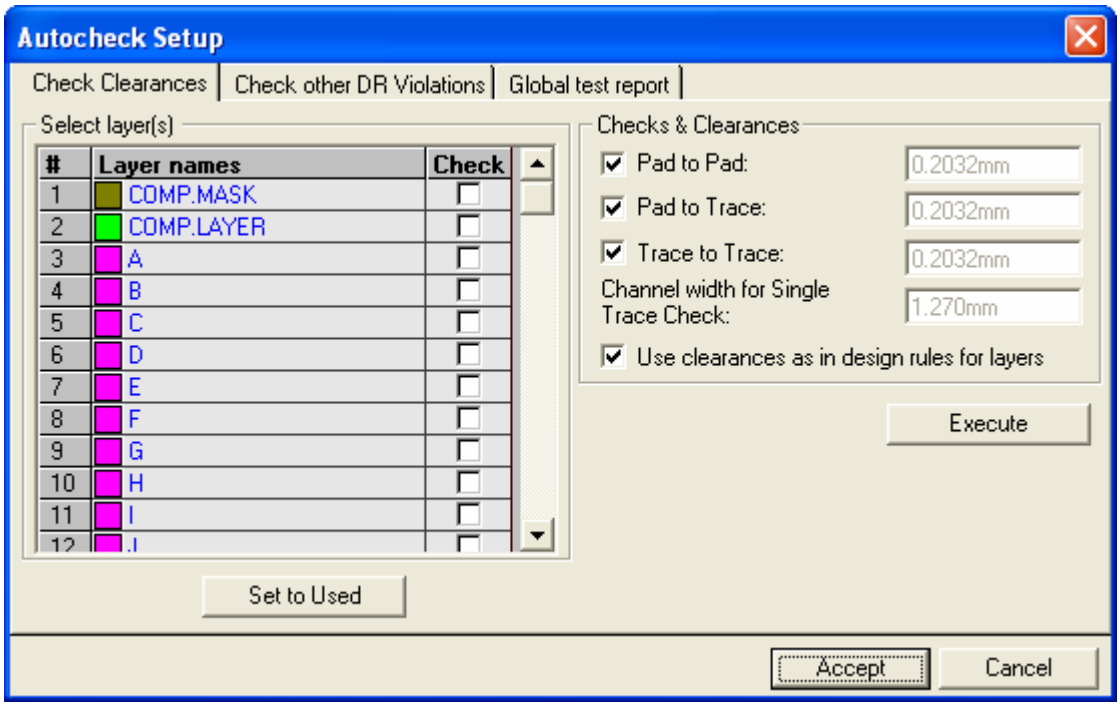
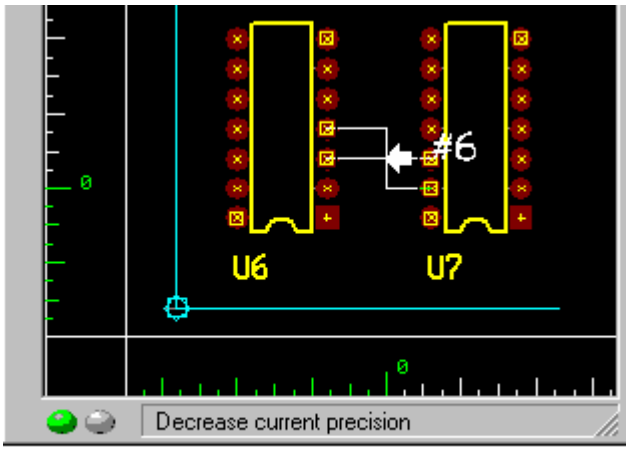


Fig 8.13

OR

After selecting the layers from autocheck menu, follow the steps given below:

1. Select  Block Edit tool from Tools toolbar.
2. Select the first function tool  Check Clearance in Block and draw where the clearance has to be checked. To test clearance for the whole board use its option tool  Check Clearance on whole Board and click on the board.
3. System displays a label ERR# to highlight the type of error, it had encountered. The following are the error number generated:
   - ERR1- pad too close
   - ERR2- pad on pad
   - ERR3-pad/trace/items too close
   - ERR4- pad on trace items
   - ERR5- trace/ item too close
   - ERR6- trace/ item x-ing(crossing)
   - ERR7 – Shortcuts to copper pour:
   - ERR8- non orthogonal trace



Trace/ Item crossing -Error #6

The color of the label ERR# indicates

which layer the error is located. The encountered type of errors may be viewed using the menu **View/ Errors/Display errors**. The statistics may be obtained from the menu **Info/ Errors**.

Following is an example of ERR labels generated after an autocheck is performed on the board.

Board Analysis

Various factors like component placement and routing may influence the working of the circuit. Different types of analysis may be performed on the designed PCB to find out how these factors influence the functionality of the circuit. There are plug-in tools like **Thermal Analyzer, Electromagnetic Analyzer** and **Signal Integrity analyzer** for analyzing the thermal, electromagnetic and signal integrity effects on the board.

Refer Chapter 9: for more information.

Miscellaneous

Layout Package

Generally, layout packages are formed as a result of packaging of symbols in the schematic editor. If necessary, new packages may be created and added to the circuit while editing the layout. If this is to be on the schematic diagram, the part added must have both the symbol and the package.

Part description contains all information about layout view (package) and schematic view (symbol(s), packaging and pinout) of the component. There are also parts, which do not have symbol information prohibiting them from taking part in back annotation.

 *Parts, which do not have symbol, are not back annotated to Schematic, but part containing both symbol and package is back annotated to the Schematic.*

Layout Component as 'Package'

It is also possible to create new layout components using only packages as reference but referred as parts. In this case no information of symbols will be passed to schematic diagrams. One of the main purposes of this mode is to create layout components, which are not required to appear on the schematic diagram. For e.g. it may be needed to reserve space for screw holes in the PCB board as shown in Fig.8.15.

 *These parts are not annotated to Schematic*

There is no explicit function to create holes for fixing screws. A package may be created or an existing package used whose pads represent holes while generating NC drill list.

{bmct tmp1.bmp}The component(s) placed by either of the tools (Browser/ Explorer) has component name (E.g.: U1) displayed by the side of the component.

Selecting Objects

Refer selecting objects in Schematic Editor Page

Change reference

☛How to change reference?

Purpose: To change the reference of a component placed on the editor.

Operation: Open the Library Browser or Explorer and click on the component present in the search list. Press Alt key and drag the component from the Browser or Explorer to the editor and move anywhere over the component, which is required to be replaced. Now, release the mouse. The reference of a component may also be changed in the following way: Select (press Ctrl and click on the component) the component and right click anywhere on the workspace. A menu pops up from which click Properties/ Layout Component Property window pops up where various option are provided for the bulleted component(s) and its entries. To change the reference, type the required Part name in the Part field. Press enter or click the next row. The part on the schematic editor is replaced if the component name typed is available in the Library.

Only Components that are not packed may be changed. If it is packed, the reference may be changed in Layout else unpack the component and proceed with changing reference.

Renumber Components

After the PCB layout design is complete, it is a normal practice to renumber the components. This is required, because, while placing the components on the board either manually or automatically, the optimization of connecting length is the governing criterion. However, for the board to be assembled and serviced, it is desired to have an orderly sequence in component naming. There is an automatic function to perform this. The numbering sequence may start from the top of the board, move in an ascending order to the right in a row, or start from top, and then move down in a column like:

	ROW ORIENTED				**COLUMN ORIENTED**			
	U1	U2	U3	U4	U1	U3	U5	U7
BOARD TOP								
	U5	U6	U7	U8	U2	U4	U6	U8
					OR			
	U5	U6	U7	U8	U2	U4	U6	U8
BOARD BOT					OR			
	U1	U2	U3	U4	U1	U3	U5	U7

- Select the Autorenumber function from the Auto submenu.
- Define name prefixes of components to be renumbered. If all the components are to be renumbered, define them one after the other.
- Set the starting point of the renumbering, by selecting the board corner.
- Set the direction of numbering, viz. column-oriented or row-oriented.
- Set the point on the component that is to be considered as coordinate reference. Normally pin 1.
- Set the channel width. This will consider all components, whose pin 1 or the reference defined in step 5, falling within this channel width, as placed in same column or row.
- The system automatically updates this renumbering to schematic diagram.

Chapter 9

Board Analyzers

Types of Analyzers

EDWinXP provides two board analyzers.

Thermal Analyzer

The Thermal Analyzer is intended to be used for analyzing and identifying potential thermal problems on a Printed Circuit Board. It evaluates the Temperature Distribution on a finished PCB, at steady state conditions. From this information, the designer can not only identify potential problems in the design stage itself, but also try out various solutions too - all in an interactive graphical environment. The analysis may be done with the parameters set to appropriate values. The result of the analysis may be displayed using isotherms or color mapping scheme.

Electromagnetic Analyzer

Electromagnetic Analyzer is used to predict the intensity of electromagnetic field generated by the working circuit on the PCB. An electromagnetic field develops when voltage passes through the traces on board. Once the routing of traces is complete, electromagnetic analysis may be performed on the board. The Electromagnetic Analyzer measures the distribution of the Electric Field Intensity on a finished PCB. The isolines show the distribution of the field intensity on the board. Under the electromagnetic analyzer you can perform Signal Integrity Analysis and Field Analysis.

Signal Integrity Analysis

The Signal Integrity Analyzer examines the probable distortion of high-speed signals as they pass through traces on the PCB. The results of the analysis are displayed in the Waveform Viewer. The purpose is to predict how a signal deviates from its ideal (or intended) behavior in a real-world setting.

Field Analyzer

The Field Analyzer is a tool for studying the electromagnetic fields that are created when power and/or signal traces on the board are energized. The results of the analysis may be view as a color graph, isolines, 3D-wire mesh graph, etc. It must be particularly mentioned that, just as with the other two tools, the Field Analyzer does not make any decisions or suggestions about the proper functioning of the design. The Field Analyzer predicts the variations in the selected field, due to electro

magnetic properties of physical connections (traces), within a spatial area and time frame specified by the user.

Steps for Thermal Analysis

To understand the thermal analysis, an example project COUNTER.EPB is used.

1. Right click on the task  **PCB Layout** in the Project Explorer to unfold a list of functions. Clicking on  **Board Analyzer** in this list opens up this module.

2. From the drop down list of the File menu of Project Explorer, select **Open Project** and select a project. Load the project **COUNTER.EPB** from **\Job** directory.

3. Select the **Thermal Analyzer** tab.

4. Right click on the workspace and select the tool  **Display Parameters**. Or select **Analysis/ Settings** to open the settings window and click the Display Options tab (Refer Fig.9-1). Set the raster to a minimum value (0.025”) and set the Isotherm density to (0.1°C) for better analysis result.

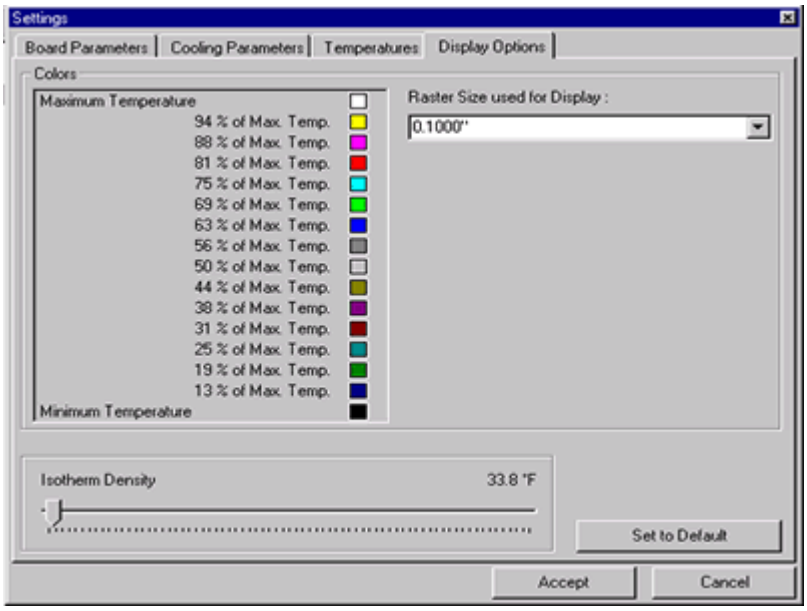


Fig. 9-1

5. Right click and select the tool  **Board Parameters** (Or select from the Analysis menu). The board parameters are set to the default values by clicking the **SET TO DEFAULT** button as shown in Fig. 9-2.

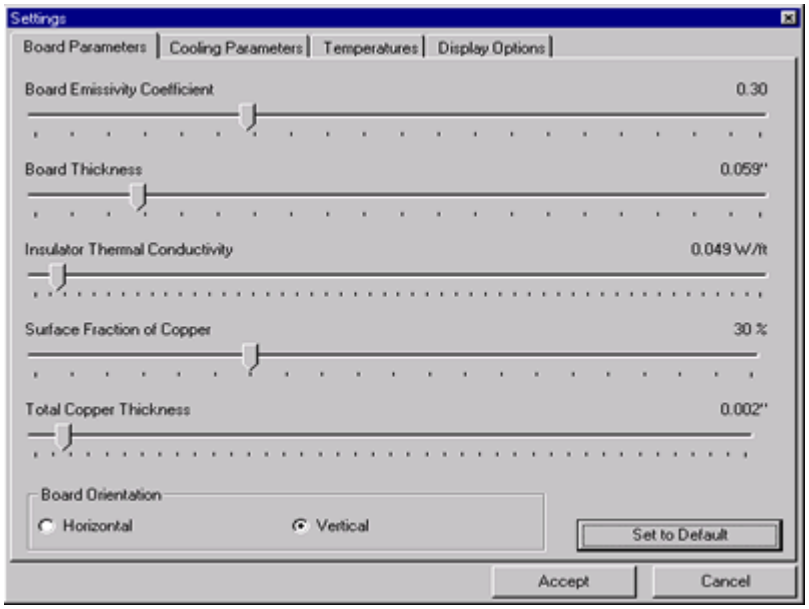


Fig. 9-2

6. After supplying necessary parameters, right click and select the tool  **Execute** to execute the analysis. The result is displayed in the form of isotherms and color mapping of the board may be viewed by switching on the option **View / Analysis Results / Colored board.**

7. The analysis result is as shown in Fig. 9-3.

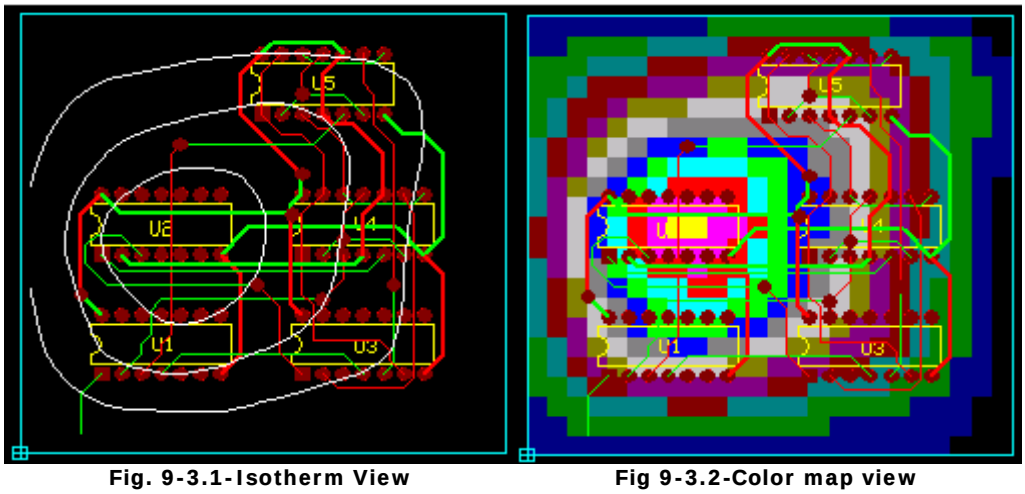


Fig. 9-3.1-Isotherm View **Fig 9-3.2-Color map view**

8. From the result it may be easy to identify the most heated component; a heat sink may be used for this. To simulate the heat sink effect, select the tool  **Component Parameters** and click on the component. A **Thermal Parameters** window pops up where you may set the cooling parameter for the component. Enter the **Thermal Resistance of Heat sink** (e.g. 1.2°C/Watt) value and click OK (Refer Fig. 9-4).

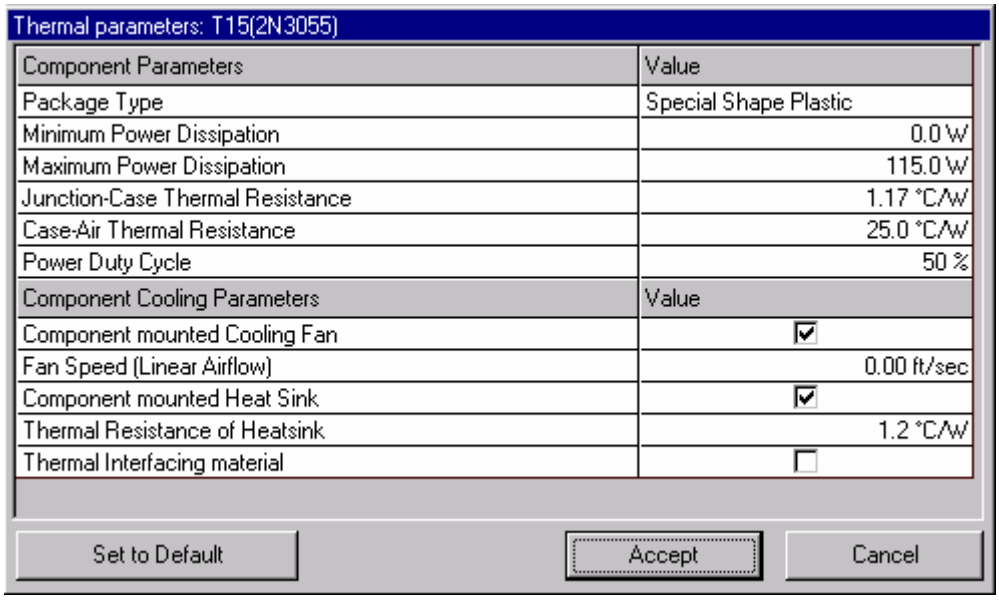


Fig. 9.4

Repeat the same step for all other components and execute the analysis again. You can notice the change in the isotherms after conducting the thermal analysis.

9. Labels may be placed to display the temperature at various points on the board. For this right click and select the tool **Set / Delete Label** and click on the board at required locations. Label gets tagged to the cursor. Now drag the mouse to place the label at proper place.

To delete the isotherm label click again on the label.

Steps for Electromagnetic Analysis

To understand the thermal analysis, example project SPICDEMO.EPB is used.

1. Right click on the task **PCB Layout** in the Project Explorer to unfold a list of functions. Clicking on **Board Analyzer** in this list opens up this module.

2. From the drop down list of the File menu of Project Explorer, select **Open Project** and select a project. Load the project **COUNTER.EPB** from \Job directory.

3. Select **Electromagnetic Analyzer** tab

4. Repeat the same procedure for the other two nets UN2 and UN5 and include these two nets also for analysis. Enter the voltage and frequency value for each net and add to the list.

For example;

UN1 - 5V, 1MHz
UN2 - 5V, 1MHz
UN5 - 5V, 1 KHz

5. If you select the SET TO DEFAULT button, the default parameter gets loaded into the text boxes (Refer Fig.9.5).

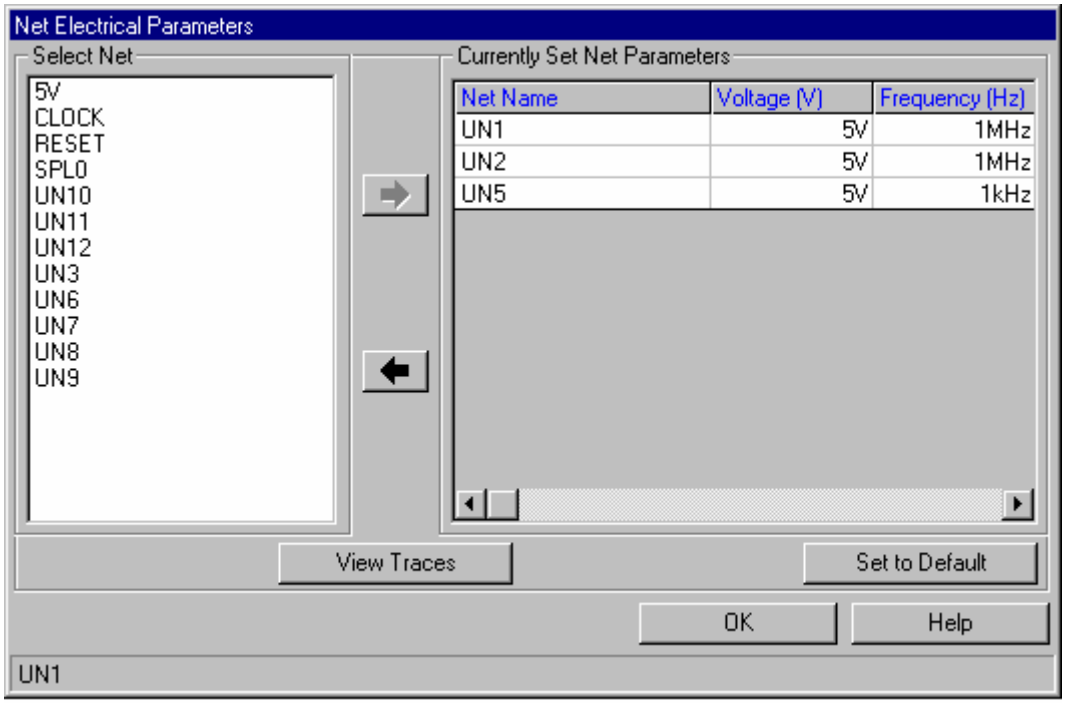


Fig. 9.5

6. View the electrical parameters of the trace from point to point using the VIEW TRACES button (Refer Fig. 9.6).

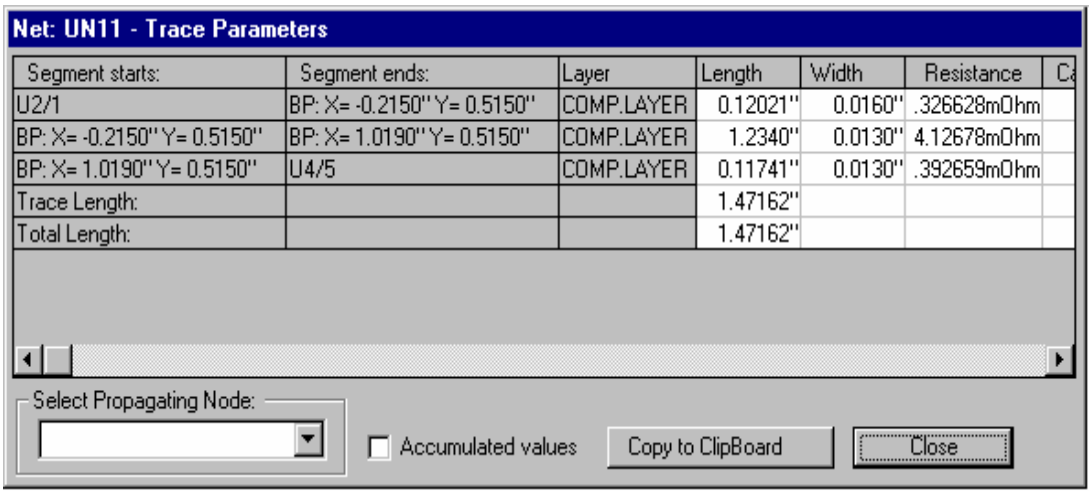


Fig. 9.6

7. After adding these nets you may execute the analysis directly. For this right click and select the tool **Execute Analysis**. The result is displayed in the form of isolines. Color mapping on the board and may be viewed by switching on the option Colored board under **View / Analysis Results** menu.

8. The analysis result is as shown: The Maximum and minimum field intensity locations are shown in Fig. 9.7.

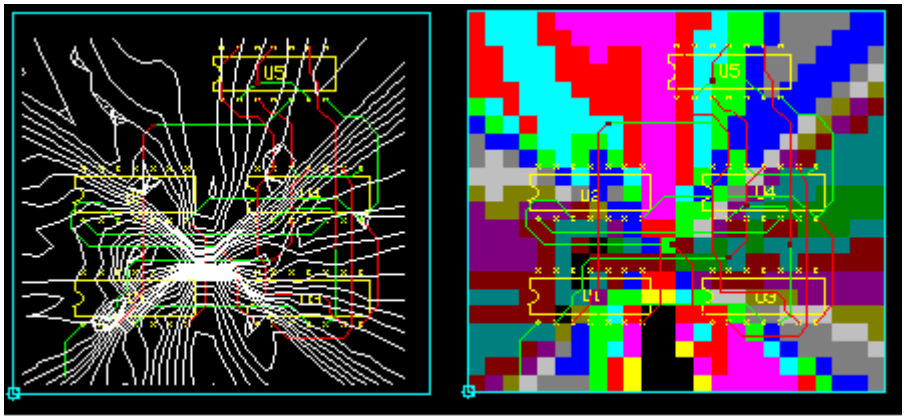


Fig. 9.7

9. Labels may be placed to display the field intensity at various points on the board. For this select the tool Set/ Delete Isolines and click on the board at required locations. Label gets tagged to the cursor. Now drag the mouse to place the label at proper place.

To delete the isoline field label click again on the label.

Steps for Signal Integrity Analysis

Under normal working conditions, signals propagate from some pins of the components in the circuit (technically called **Driver Nodes**), through the interconnecting traces and into pins on the same or other components (called **Receiver Nodes**).

Traces have electrical properties like resistance, capacitance and inductance. These parameters are distributed all over the trace and are not concentrated anywhere. The electrical properties of the traces influence the signal as it passes through. For signal frequencies below 1MHz, and trace sizes normally encountered, these influences are so small that they can be safely neglected.

However, above 1MHz, especially close to the GHz range, the electrical parameters of the traces begin to exert significant influence on the signal as it passes through. In this situation, the trace is said to be behaving as a Transmission Line. Sometimes,

the effect is so severe that the signal that comes out of the trace is totally different from the one that entered it. As the switching speed of modern digital electronic parts goes well into the MHz ranges, signal integrity problems become more of a concern.

This analysis detects the degree of distortion of the signal from its ideal behavior while it passes through the trace and graphically presents the comparison result with the help of the **Waveform Viewer**.

To understand the thermal analysis, example project Counter.EPB is used.

Signal Integrity Analyzer is invoked from within the Electromagnetic Analyzer. Right click on the task  **PCB LAYOUT** in the Project Explorer to unfold a list of functions. Clicking on Electromagnetic Analyzer in this list opens up this module.

1. From the drop down list of the File menu of Project Explorer, select Open Project and select a project. Load the project COUNTER.EPB from \Job directory.
2. Right click on the workspace and select the tool  Signal Integrity and click on any of the trace, which is to be analyzed.
3. Now select the net UN6 that connects the nodes of U4/8, U4/12 to U5/3. A window pops up where you may set all the parameters for simulation. To check the integrity of an electromagnetic signal while it passes through this trace, go through the following steps.
4. All nets are displayed in the frame Available Nets. Select UN6 from the list and click  . The segment nodes of the selected net get displayed in the frame Selected Nets. Right click on the node U4/8. The selected node may be set as driver node. From the drop down 'Function' select Square Pulse having zero rise and fall times. The electrical properties of the trace will influence the signal as it passes through it and this is shown in the respective columns.

 *If the user wishes to use the same input conditions used in Simulator, the item PWL (Recorded) must be selected from the dropdown list. This can be recorded using the Record Output as PWL file tool in Oscillograph (Mixed Mode Simulator / EDSpice Simulator).*

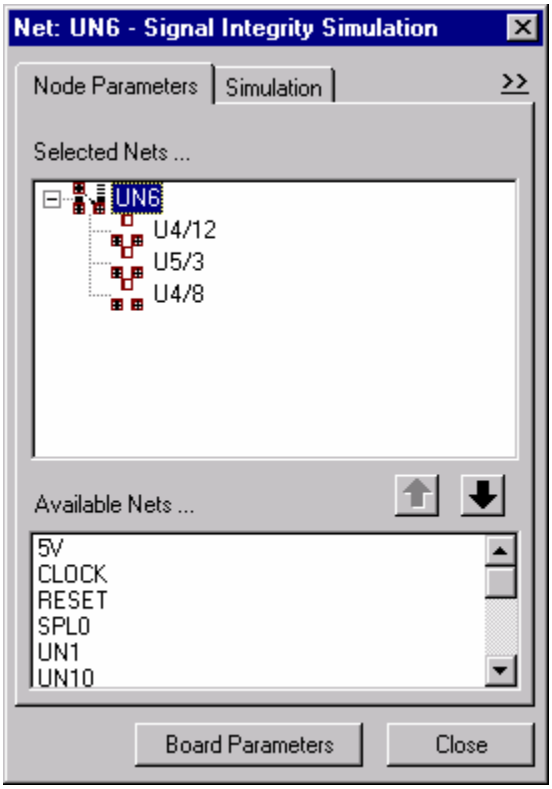


Fig.9.8

5. Set the following parameters.
   Max voltage to 5V and
   T L->H = 0
   T H = 1us
   T H-> L = 0
   T L = 1us

To set these parameters, click on the respective cell and enter the values and then press the ENTER key.

6. The Technology list allows selecting different technologies for both Input and Output pins for the analysis. Select TTL technology from the drop down. The Rout, Lout and Cout parameters are automatically read from the file, Families. EMA that resides in the \SYS directory. The values may be edited by clicking the corresponding box. N/A text denotes that they are not applicable for this family.
7. Next set U4/12 and U5/3 as the Receiver nodes. Set TTL technology to the receiver nodes. Check the check box corresponding to Test Points. The Test points allow to display the output of the selected node in the waveform viewer. If no test point is selected then output waveform alone is displayed on the waveform viewer. Selecting the Driver node and Receiver node automatically selects the interconnecting nodes traces too.

Simulation may be done for either any one of the selected nets or all of them together. This makes it possible to check not only the effects on each trace considered in isolation but also of interactions between various traces on the board.

8. The Trace Segment parameters of the driver node may be viewed by clicking on Show Trace Segments (Refer Fig.9-9). Test points may be placed on any of the bend points on the trace segments between the input and output pins by marking the test point check boxes.

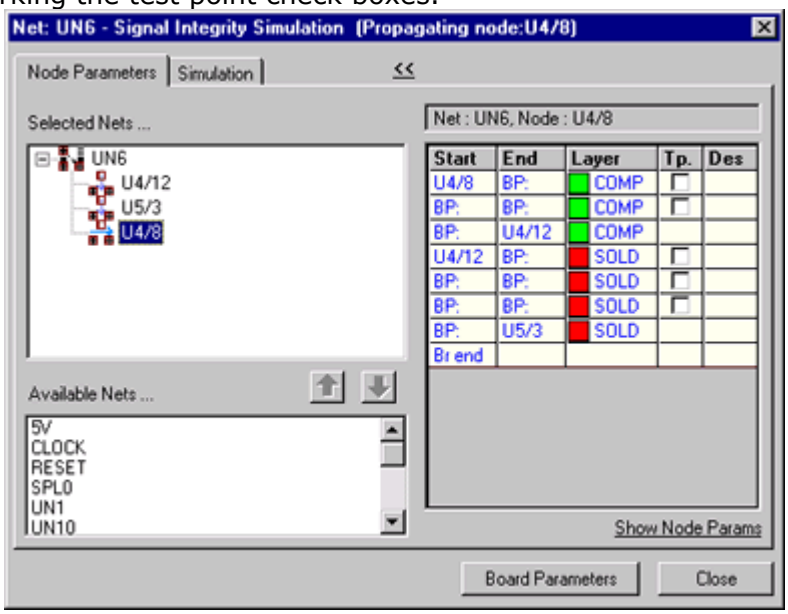


Fig. 9.9

9. To execute simulation, Start time and End time of the simulation as well as the sampling time interval must be specified. This corresponds to the parameters Start time, Time limit and Time step (Refer Fig. 9.10).

10. The ***CALCULATE*** button allows to calculate the maximum time limit and will update the text box Time limit. Here the time step is set to 1ns and Time limit to 2us.
11. Various parameters of the board that influence its electromagnetic behavior may also be specified using the button ***BOARD PARAMETERS***. This opens a window that allows to set the parameters for the board such as thickness, electrical permeability and total copper thickness. Click **SET TO DEFAULT** button to select the default values. All the traced layers to be simulated may be included using the button **SET TO TRACE LAYERS USED**. In addition to this it also allows to include other layers to make sandwich. To select multi layers use CTRL button and then click the button MAKE SANDWICH. The dielectric in between the successive layers may be edited by clicking the corresponding cell. Click ***ACCEPT*** to accept the values.

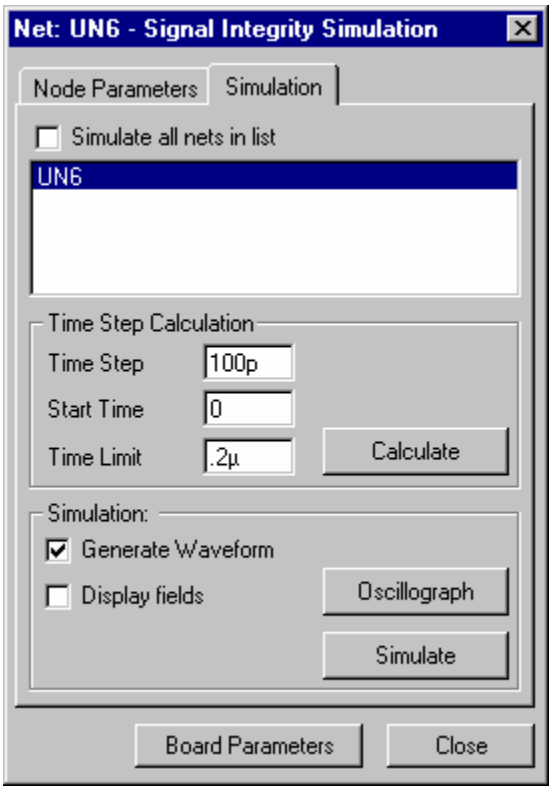


Fig. 9.10

12. The check box '**Generate Waveform**' should be checked. The result is displayed in the waveform viewer. Checking the option 'Display Field' will invoke the Field Analyzer. (See the next section for notes on Field Analyzer). Click the ***SIMULATE*** button to process the simulation. The in for one wavelength and a time step of 1ns gives the following result as shown in Fig.9.11.

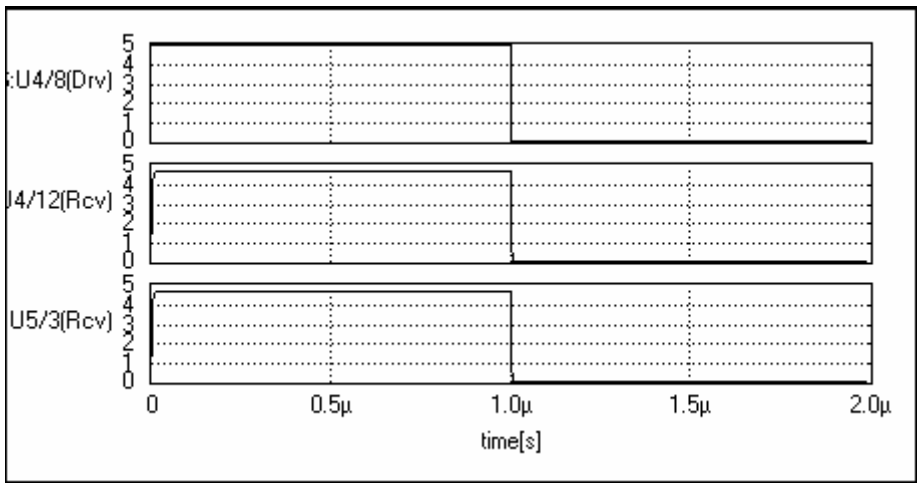


Fig. 9.11

13. Zooming up the particular areas as shown below may identify the distortion levels. You will observe that the signal that comes out of the trace is different from the one that entered it (Refer Fig.9.12).

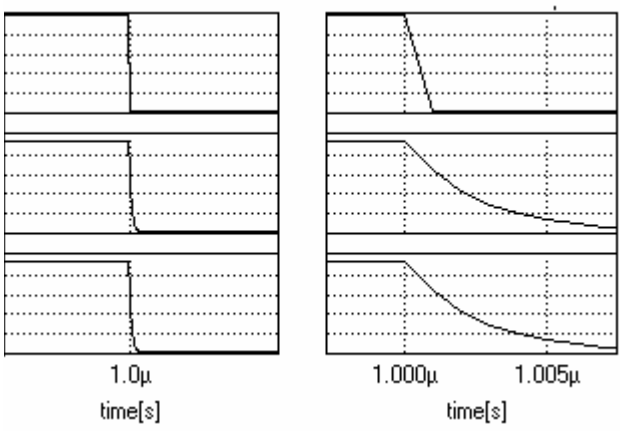


Fig. 9.12

Tip: To zoom a particular area in the diagram, press SHIFT + B. Click the left mouse button and drag it to enclose the area you wants zoom. On releasing the mouse button you get the diagram enlarged.

By consequently changing the start time and time step you will be able to view the distortion levels at various points.

Field Analyzer - Operation

The field analyzer is invoked from the **Signal Integrity Simulation** window. Follow the steps given for Signal Integrity Simulation to select the trace, receiver nodes, driver nodes, etc. Check the option '**Display Fields**' in the **Signal Integrity Simulation** window and click the **SIMULATE** button to open the Field Analyzer.

From the Field analyzer window, click on the Run Simulation button to begin the Analysis. The maximum and minimum values of the field at each instant of analysis time, within the specified range are displayed. The blue status bar shows the time elapsed and the percentage of total analysis completed.
The simulation may be interrupted (and continued later) at any desired point by using the Pause button. This could be very useful to study particular points of interest within the specified time interval. In order to continue the interrupted analysis, simply click the Continue Run button.

Using the Stop button may stop the simulation. However, doing so will discard the current simulation and it cannot be continued from that point forwards.

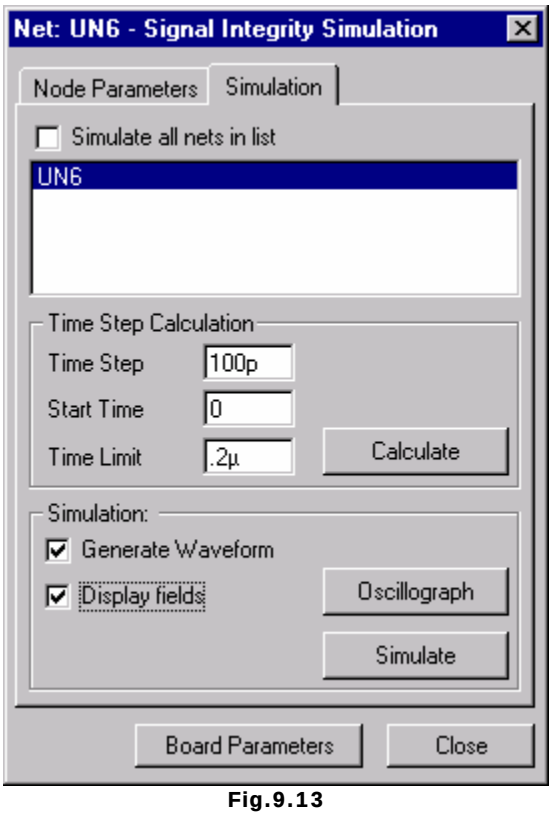


Fig.9.13

Once the analysis starts, information about the field is dynamically presented in two ways:

1. The Field display area will show variation of the selected field type using the graph type specified.

2. Depending on the current choice, the Waveform display area will show either
    a. The time variation of the amplitude of the selected field type or
    b. It's spectral content at that moment.

Maximum values of the selected field type within the entire graph area as well as at the probe location are shown in the status bar. These values are updated at every time step specified.

If AutoScaling has been selected, the maximum values displayed as well as the scales of the graphs are automatically updated. On the other hand, if AutoScaling has been turned off, these values are clipped at the values specified. (In other words, values higher than those specified are ignored.)

Using Field Analyzer

The Field Analyzer is started from within the Signal Integrity Analyzer. Before invoking it, the following settings must be done from within the Signal Integrity Analyzer window:

- Select the Net(s), which is to be simulated.
- Select the Driver Node(s) for each Net.

For each Driver Node, specify all required parameters such as Signal Function, Technology, Resistance, Inductance, Capacitance, Voltages, Frequencies etc.

- Select the Receiver Node(s) for each Net.

For each Receiver Node specify Technology, Resistance, Inductance, Capacitance, and Test Points etc.

- Specify the Time Step, Start Time and Time Limit for the Simulation.
- If necessary, specify the required values for Board Parameters.

The Field Analyzer will use these values to perform the simulation.

In order to start the Analyzer, make sure the Display Fields check box is turned on. Clicking on the Simulate button will now bring up the Analyzer window. The Display area will show the following:

1. The board outline along with the layout of the trace selected for analysis, and
2. A waveform display area for showing the Time or Spectral variation of the selected field during Analysis.

A few further settings are necessary within this window before the actual Analysis can be performed. Proceed as follows:

- **Set Graph Extent**

Size of the square covered by graph
Use the Zoom-Up and Zoom-Down buttons for setting this value. Click Graph Modes to set the graph extent.

- **Specify density of the isolines**

Increasing this value will result in a more detailed presentation of results. However, the increased amounts of data generated will result in a slower analysis. Click Graph Parameters to set isoline density.

- **Set the Color graph precision raster Size**

This value is used to set the precision with which the field values are calculated. Higher values will have greater precision, but take more computing time. Click Graph Parameters to set precision raster of the color graph.

- **Set the Color graph display grid Size**

This value is used to set the smoothness of the colored graph. Higher values will show smoother variations. Click Graph Parameters to set display grid of color graph.

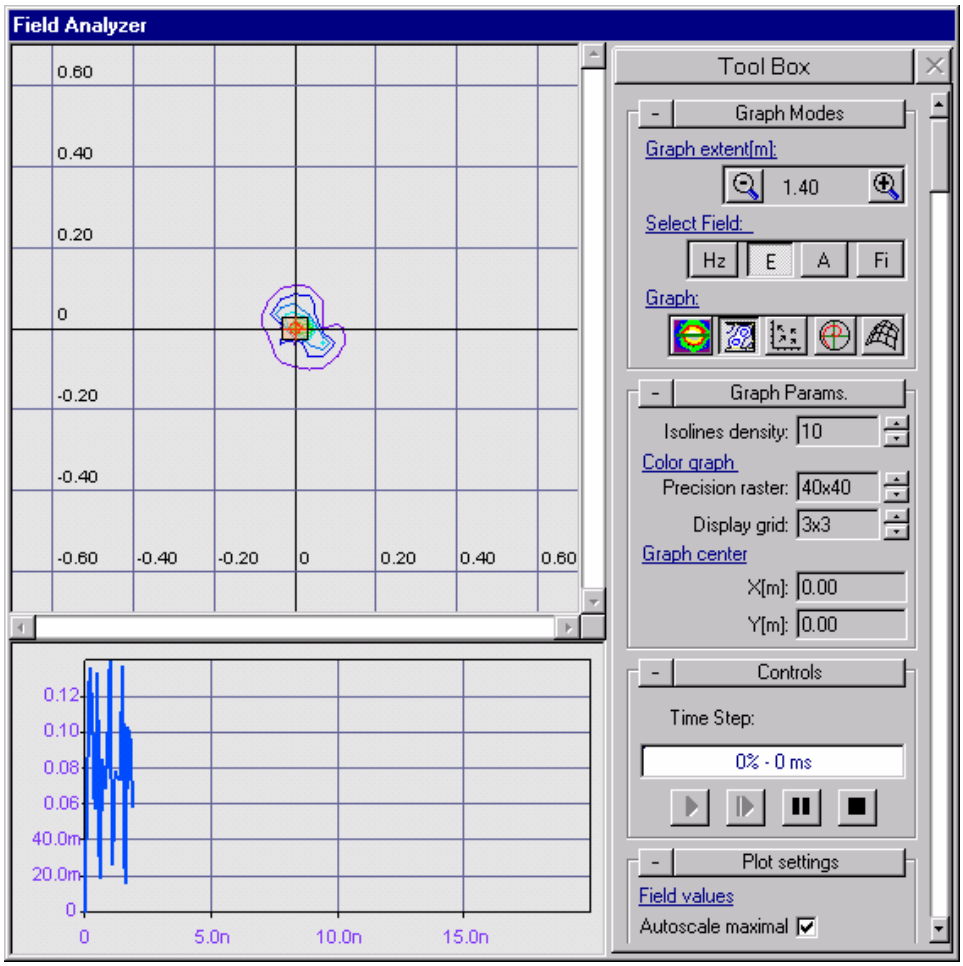


Fig.9.14

- **Specify the Time Step value**

This value controls the speed with which the analysis is performed. The default value is the same as the value specified in the Signal Integrity Analyzer. Any one of the various multiples of this value, as shown in the drop-down box may be selected. Click Control to set the time step value.

- **Relocate the display of the board**

The location of the board within the display area can be set using the scroll bars

- **Specify the type of field you wish to study and the manner in which it should be graphically displayed.**

Any one of four types of field distributions may be selected for analysis. These are

1) Electric field distribution
2) Magnetic field distribution
3) Scalar Magnetic Potential distribution
4) Vector Magnetic Potential distribution

Click Graph Modes to set the type of field distribution.

The fields are obtained by a solution of Maxwell's Equations of Electromagnetism. These are given below:

$$\nabla \cdot \vec{H} = 0$$

$$\nabla \cdot \vec{E} = \frac{\rho}{\varepsilon_0}$$

$$\nabla \times \vec{H} + \vec{j} = \varepsilon \cdot \frac{\partial \vec{E}}{\partial t}$$

$$\nabla \times \vec{E} = -\mu \cdot \frac{\partial \vec{H}}{\partial t}$$

These four equations completely characterize the Electromagnetic field due to the characteristics of signals selected for analysis. Using the parameters that have been specified, these equations are built up and then solved to arrive at a distribution of the field pattern. The equations are iteratively solved over the time period specified so as to obtain the dynamic variation of the field.

Each one of these fields may be viewed in any one of the graph options available. (Depending on your choice of field, some of the Graph options may not be available.) These are:

Colored graph	It shows the predicted variation of field intensity by coloring areas at the same value with the same color.
Isoline graph	It uses isolines to represent the field. Areas at the same field intensity fall on the same line.
Field direction graph	Directed Lines (Arrows) are used to show the direction of the field at each point. Applies only to electric field graph
Polar coordinates graph	It shows the maximum field intensity in a given direction, with the card placed at the center.
3D wire mesh graph	A 3-dimensional, wire mesh view of the field variation is shown.

Click Graph Modes to set the type of graph.

- **Specify the location of the Probe**

The probe is represented by means of a small red circle with centre lines. By default it is located at the origin of the axes. It can be positioned at any point in the field display by clicking at that point.

Chapter 10

Fabrication Manager

Introduction to Fabrication Manager

Fabrication is the last stage of the electronic design process. The PCB information is converted into ASCII output files – GERBER (.gbr), NC Drill (.ncd), PCB Assembly Outputs Generic (.pck), IPC-D-355(.355), Bare Board Testing Generic (.bbt) and IPC-D-356A (.356) which is given as input to the machines for creating the hardware.

This chapter explains the fundamentals in generating these ASCII output files. Fabrication Manager also provides a GERBER Viewer to preview the artwork of the output files. The section below provides an overview of the structure and working environment of Fabrication Manager.

Fabrication outputs

The Fig.10.1 shows the outputs generated using Fabrication Manager.

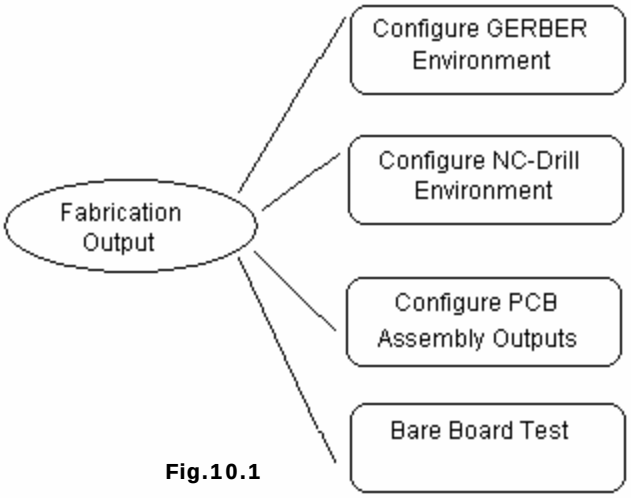


Fig.10.1

The major Fabrication tasks involved in PCB design are as follows.

Fabrication Tasks

- Optional creation of Copper Planes and Copper Pour Areas
- Adding dimensions and notes
- Printing layout documentation drawings
- Extracting NC-drill data to disk files or paper tape
- Editing, dimensioning and printing of drill templates
- Editing and printing of layer artworks

- Generation of artwork data files in GERBER ASCII format
- Preview of artworks of GERBER ASCII files
- Generation of disk files containing generic data for Pick & Place machines
- Generation of disk files containing bill of materials

Before going in detail with Fabrication Manager, refer Fabrication help for the tasks listed above.

Fabrication Manager

The section below provides information on how to invoke Fabrication Manager and describes the general outlook of the working environment.

☛How to start Fabrication Manager?

Click on the task  **PCB Layout** in the Project Explorer and adopt either of the following methods.

- Right click on the particular task(here it is  PCB LAYOUT) and select the function ( Fabrication Manager)
- Select the particular function ( Fabrication Manager) from the task list OR from the task toolbar.

The Fabrication Manager window opens with a default board size and gets aligned with the Project Explorer to fit the screen.

General outlook of Fabrication Manager

The Fabrication Manager presented below contains menus and toolbars that control the objects placed on the workspace. Most of the functions are similar to Layout.

File

The File menu item provides the main interface to generate the final outputs. The validation outputs can be generated on printers or laser jet devices. As standard Windows drivers are used by this program, standard Windows commands may be used to get the outputs. However, application oriented interface dialog boxes are provided by the program.

File (Print)
Pops up a window "Preview" that allows previewing the contents on the workspace. It also provides the option to print pages in scales from 10:1 to 1:10 and to set the X & Y offsets.

File (Load Notes)
Opens Select Board Notes to Load window that allows loading notes from another file into the current project. The path and name of the file (*.ebn) of the saved notes are entered in this window, from where it may be extracted.

 *This option is active only when Tools/Notes are active.*

File (Load Template Notes)
Opens Select Template Notes to Load window, which loads the template notes to the current project. The path and name of the file (*.etn) of the saved notes are entered in this window, from where it may be extracted.

 *This option is enabled only when Tools/ Template (Notes) is active.*

File (Load Graphic Import)
Opens 'Select Graphic Imports to Load' that allows loading the graphic data to the current project. The path and name of the file (*.gie) of the saved graphic imports are entered in this window, from where it may be extracted.

 *This option is enabled only when Tools/ Graphic Imports or Tools/ Reconstruct from Graphics is active.*

File (Save notes)
Pops up a window 'Save Notes' to save the notes present in the current project as a file with *.EBN extension. The path and name where the file is to be stored may be set in this window.

File (Save Template Notes)
Pops up a window 'Save Template Notes' to save the notes present in the current project as a file with *.ETN extension. The path and name where the file is to be stored may be set in this window.

File (Save Graphic Imports)
Opens a window "Save Graphic Imports" that saves the graphic data. The path and name of the file (*.gie) is entered in this window.

 *This option is enabled only when Tools/ Graphic Imports is active.*

File (Gerber/ Excellon/ DXF/HPGL Viewer)

Opens Fabrication Graphics (Gerber/ Excellon/ DXF/ HPGL) Viewer & Import window that permits the user to import and view the Gerber ASCII files, DXF, HPGL, and Excellon files for viewing and validating purposes before photoplotting.

Special function incorporated in the viewer converts imported data to the categories that may be edited in Fabrication Manager prior to reconstruction of projects from graphics. The viewer also has the capability for automatic distribution of imported data to most suitable category.

File (Copy Screen to Clipboard)
Copies current screen contents to the clipboard.

File (Copy Block to Clipboard)
Copies the contents of the selected block to the clipboard.

File (Exit)
Allows exiting from the currently working module. It also saves the settings made on the workspace for e.g. the view settings, Preference settings etc…

Edit

The Edit menu allows the user to carry out standard edit operations on various objects placed on the workspace. The menu items such as cut, copy, paste, delete, select all and properties are enabled only after selecting (bulleting) objects on the workspace.

Undo	Reverses the last operation done or deletes the most recently placed object.
Redo	Redo reverses the undo action.
Cut	Removes the selection of the active page and places it on clipboard.
Copy	Copies the selection of the active page and places it on clipboard.
Paste	Inserts the contents of the clipboard at the insertion point on the page and replaces any selection. Paste option works only if a cut or copy operation had been done earlier.
Delete	Deletes the selected object without putting it on the clipboard.
Select All	Selects all texts and graphics in the active window.

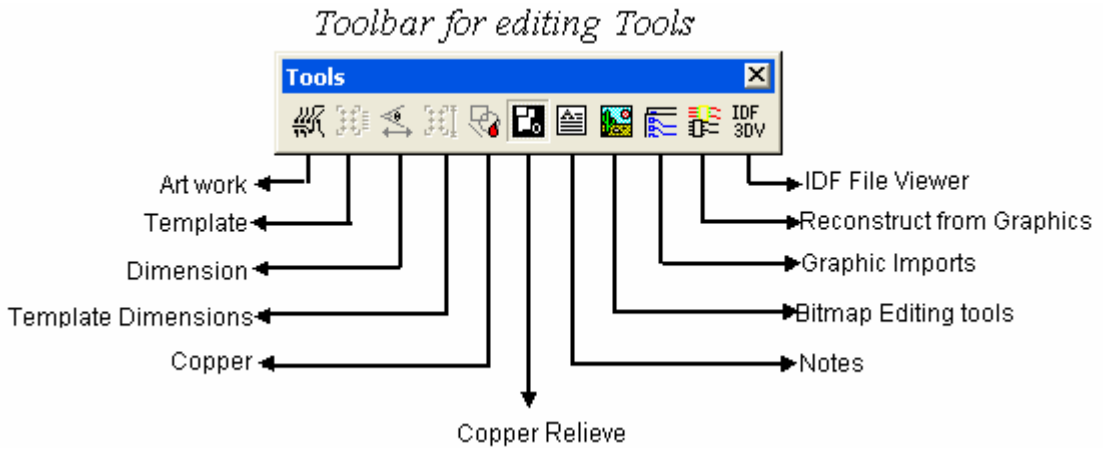
Properties
Displays the properties of the selected (bulleted) objects. Depending on the objects selected, the contents of dropdown list of the properties menu varies. Select this option from the edit menu after bulleting the objects. Properties may also be obtained by right clicking on the selected (bulleted) objects. On right click a window pops up, from which the properties of different objects may be viewed. Some of the properties are mandatory.

Bullet
This feature enables to select (selection by bullets) only a particular group of objects from the selected objects so that the properties of the selected group of objects may be edited. Especially useful when all objects on the workspace is selected.

Layer
A maximum of 32 layers in a multi layered card is supported. These layers are logically divided into two groups of 16 layers each; the first 16 layers are referenced

as Component side and the other 16 as Solder side. This menu allows the user to select the various layers of the board. The layers may be selected from the solder side as well as component side.

Tool
Displays a list of menu items and is present in Schematic, Layout and Fabrication Manager. The menu in this list differ in each editors and when selected allows entering into main object oriented function.



Whenever a tool/ menu is selected, its corresponding function and option toolbars are displayed, provided these toolbars are made visible using View/ Toolbar.

Tools (Artwork & Pwr/Gnd Planes)
This is merely a print preview of GBR files and various settings in preview can be set. The artwork of a printed circuit board is the actual display of the various copper routes, padstack, pinholes, etc. The design data may be viewed layer by layer as it is got on the photoplotted film or pen plotted artwork. This menu option must be active to view the various layers of the design individually. In order to view any of the layers, use the Layer pull down menu and select the required layer. The artwork for that particular layer may be viewed as it appears on the film.

Creation of Copper Pour Area

Refer page -221 (4th point).
On the artworks, Copper Pour Areas are drawn as filled polygons. All traces inside are drawn with airgaps. Pads not belonging to net to which given Copper Pour Area connected is also drawn with airgaps. Pads which are nodes in reference nets and are inside connected Copper Pour Area are drawn as HRF pads as shown in Fig10.4. If they are outside Copper Pour Area, then they are drawn as any other pad.

When the **Artwork & Pwr/Gnd Planes** menu is invoked **"Select layers for preview"** opens where the required layers may be selected and click ***ACCEPT***. The artwork as shown in Fig.10.4 appears in the workspace.

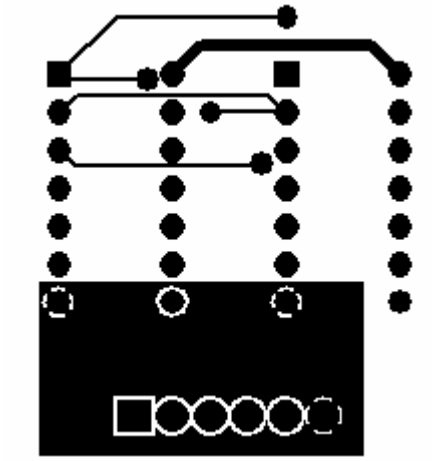


Fig.10.4

Tools - Template [notes]
This menu option is active only when the drill data has been generated using the NC Drill menu. It allows adding manufacturing notes to the template data.

Tools - Dimensions
This menu option provides tools to add dimensions to the layout. For this first define the end points between which the dimension information has to be provided. Contact points are used to define the graphic entity reference points. Dimensioning may be done using the function tools displayed. When this menu option is active the Select Layer option is disabled in the Layer pull down menu since dimensions are usually placed on the Component Print and Solder Print layers. Hence selecting Comp Side and Solder Side items allow to place the notes on Comp. Print and Solder Print layers respectively.

Tools- Template [dimensioning]
This menu option is active only when the drill data has been generated using the NC Drill menu. This template is used as a drawing by the PCB manufacturer to inspect the board drilling, hole size and board dimensions. This menu option provides tools to dimension the template (drill data) created using NC-Drill generation

Tools - Copper
Copper function enables placing of conductive elements on trace layers. Conductive elements may be either of the graphic items - Lines, Arcs, filled and unfilled Circles and Rectangles or a new type of "item" - Copper Pour Areas.
All graphic items are just plain copper. They may or may not be logically connected to nets. Wherever they are placed on the board they may be used to combine copper planes. Each of them may have an airgap defined. They may also be used to draw boundaries of hatched areas, which are in the same category. They are always drawn or photoplotted and any other object placed above them will melt within.

Tools - Copper Relief
This option switches the system to the tools for creating/ editing copper relieve areas. Copper relive areas may be created using graphic items such as lines, rectangles, circles, arcs, polygons etc.

Tools - Notes
This menu option provides tools to add any additional information as well as manufacturing specifications into the layout design. These tools are the same as those used for creating design notes. When this menu option is active the Select Layer option is disabled in the Layer pull down menu since design notes are usually placed on the Component Print and Solder Print layers. Hence selecting Comp Side and Solder Side items allow to place the notes on Comp. Print and Solder Print layers respectively. The following function tool allows editing the layout features.

Tools - Bitmap
This menu option provides tools to add any additional information into the layout design in the form of bitmaps. There is also an option to make these bitmaps visible on all or selected layers of the layout design.

Tools – Graphic Imports
Due to some ambiguity in interpretation of imported graphics or because of necessity to add changes to artworks some elements in categories have to be edited. Editing graphics in Import categories is similar to editing other PCB elements like Notes or Copper. Option is provided to select category for edition. Only element belonging to selected category may be edited at the time but visibility of other categories may be switched ON and OFF.
Editing functions allow to add new elements to category, as well as changing their sizes, locations and (when applicable placement layer). Superfluous elements may be deleted. Graphics elements that were imported to wrong category because of problems with their interpretation in the import phase may be selected and transferred to desired destination.
This menu option provides tools to Import/ Edit the graphic items obtained from the artwork. The tools changes according to the selected Import Graphic Category. The categories may be selected from the Category menu or from the tool bar Layers.

Tools – Reconstruct from graphics
A separate set of tools is provided to execute this task. Tools are arranged in the toolbox in a sequence corresponding to recommended sequence of reconstruction stages. Although the program does not force following this sequence exactly, it doesn't make much sense to do otherwise. There is not much point in reconstructing traces until components are in desired locations and via holes have been reconstructed. Similarly, reconstruction of net list will not give results without traces.
On the other hand, it is up to the user to decide which objects of Project Database are to be reconstructed. For example, in case of importing PCB outline drawn using AutoCAD, only this part may be reconstructed. The rest of the Project will be designed in usual way.
During reconstruction phase the program displays PCB elements, currently in Project Database. Additionally, the program displays graphics of those categories that form reconstruction template for given type of object. Each time tool for reconstruction of given type of object is selected, the display changes accordingly.

For example, switching to reconstruction of traces causes automatic display category Trace Master. Reconstruction of components uses categories containing pad position as template.
During reconstruction phase "reconstructed" graphic elements are with some exception (pad positions) removed from import categories. It is therefore advisable to save imports prepared for reconstruction in the disk file in case some stage has to be repeated from the scratch. Functions for saving and loading of graphic import categories are available in File menu.

Tools – IDF Import 3D view
Allows importing the selected project contents in IDF standard from any mechanical CAD/CAE system to EDWinXP. To invoke this option, select IDF Import 3D view from Tools menu in Fabrication manager. A 3D Board control dialog box pops up. Here IDB and IDL files are specified and 3D view of the board will be available.

Tools - Bury Vias
Pops up a "confirmation box" to confirm burying the vias. On clicking YES, "Buried Vias Layer Sandwich map" dialog box opens. This dialog box provides information regarding vias present in the loaded project. Click ACCEPT button. The vias will appear only on the intermediate layers enclosed by the layers between which the electrical connectivity is made.

Tools - Unbury Vias
When enabled, it simply unburies the vias. This implies that the vias will now be visible on all layers except on Comp. Print and Solder Print.

Tools - Add Msng Hrf Items
Pads in reference nets may be connected to copper in two different ways. One way is to melt the pad entirely with surrounding copper. The other way is to generate so-called heat relief pads (thermal pads). In this case, the copper is partially relieved around the pin hole leaving through passes which enable connection between pin and copper. The shape and size of such relief pads may be defined by introducing so called Hrf items to the padstacks (Padstack editor). Any of the available graphic items may be used to create the copper relief areas. Normally these items are invisible and the system uses them only to generate Hrf pads of reference nets.

Tools/ Add Msng Hrf Items option maybe used to generate default Hrf items to all those pads where they are found missing.

If the padstack created does not have Hrf item added to it, the Tools/ Add Msng Hrf Items option generates default Hrf items to pads. When this option is selected 'Heat Relief items Auto generation 'window pops up'. If the radio button 'Only in padstacks with missing Hrf items' is selected, then Hrf items will be generated only for those pads where they are found missing. If the radio button **'Regenerate Hrf Items in all padstacks'** is selected, then Hrf items will be generated for all pads which belong to the Reference Net irrespective of whether they were already present or not. The Thrupath width and Airgap width for these Hrf pads may be defined in the respective text boxes.

Hrf pads are not generated for pads connected by traces on the processed layer even if they are enclosed by Copper pour area.

Tools- Add Targets Venting & Thieving areas

Opens **Artwork thieving & venting areas**, which allows to set certain PCB Fabrication Aid Items.
For PCB fabrication (especially for multi layer cards) there is a need sometimes to add certain items to artworks. These items are various graphic patterns which are

used by card manufacturer and normally do not belong to the design itself. Because of special handling required to include these items in the artworks, the whole procedure has been added to fabrication (post processing) routines.
Adding fabrication aid items affects printed and photo plotted images of the artworks, CNC-Drill outputs and Drill Templates.
Adding of fabrication aid items is optional. Each item may be selected individually.

Following are the fabrication aid items that can be added to artworks –

1. Layer Alignment Targets
2. Locating Pin Targets
3. Thieving Area
4. Venting Area
5. Coupons A and B
6. Coupons G
7. Coupons G

Fig.10.4

Layer Alignment Targets (Top/ Bottom Left/ Right)
Specifies whether to add crosswire targets at the specified corner. Bottom left, bottom right and top left corners are selected by default. These targets appear on all layers.

Thieving Area (Outer Layer)
Specifies thieving area to be added to component and solder layers (external layers) and includes empty patches for both types of targets as well as for coupons. Thieving area is used to provide uniform plating for external layers.

Venting Area (Inner Layer)
Specifies venting area to be added to inner layers. Venting area has the same size and contour as thieving area and is plotted as hatched reversed polarity pattern. The function of the hatched pattern is to provide escape channels for entrapped gases when multi layers are pressed together. It includes empty patches for both types of targets as well as for coupons.

Punch Target (Top/ Bottom Left/ Right/ Centre)
Specifies up to nine punch targets in form of crosswire with pad in the center, to be added. Punch targets are for layer registration when the manufacturer uses pin registration technique to align layers. All layers have a hole in the center of the targets and the registration pin helps to align layers when pressed together in multi layer press. The registration hole has drill diameter of 3.2 mm. Punch targets are placed inside thieving and venting areas. Default is six targets – top left, bottom left, top right and bottom right corners as well as top center and bottom center. These targets appear on all layers with exception of Component and Solder Side silk screens.

Coupon AB (2x)
Specifies whether coupons A and B are to be added. User may add two sets of identical coupons along X and Y- axis of the card. They consist of framed pattern of nine (3x3) pads with holes plus surrounding trace pattern. Assigned pad and hole diameter is the smallest found in the design.

Coupon A is used for

(i) CNC drilling

(ii) Back light test for electro less plating

(iii) Solder mask alignment and registration

Coupon B is used for testing

(i) Solder ability

(ii) Thermal stress

(iii) Pull and bond stress

(iv) Rework simulation

(v) PTH integrity

(vi) Etching (setting)

(vii) Miss registration

Coupons are provided for all layers with exception of Component and Solder Side silk screens. In solder and component side mask layers, the pad size is increased by 0.010".

Coupon G

Specifies whether to add Coupon G. It appears as chessboard pattern – square size .050" – and appears on all layers with exception of Component and Solder Side silk screens. In solder and component side mask layers, the square pad size is increased by 0.010".

This coupon is used to check:

(i) Registration of SM with pattern

(ii) Adhesion of SM on copper and epoxy

(iii) Adhesion of plated metals to base metal.

Coupon E

Specifies whether or not to add Coupon E. Coupon E is used for surface insulation resistance. The size (length) and pattern of this coupon depends on number trace layers simultaneously selected for plotting. For each layer a pair of vertically placed pads is provided, starting from top (component side). Pad pairs are repeated side by side for all other layers in the batch. Leads connected to pads move to next pair on each sequential layer.

Preferences

Provides a dropdown menu, which may be selected/ deselected to set various features. These features directly affect the working environment.

Info

The items in this menu provide information about the various objects/items created on the schematic diagram. It allows assessing free symbols, parts, packages, number of nets, etc. The necessary information is displayed in the respective info window.

View

Displays a list of menu items and is present in Schematic, Layout and Fabrication Manager etc. The menu in this list differs in each editor and when selected/ deselected toggles ON/ OFF the display of the corresponding feature on the workspace.

Fabrication

Fabrication (Setup)

Opens Fabrication Data Manager that allows to set the parameters for generating output data to Gerber, NC Drill, PCB Assembly Outputs and Bare Board Test Data Output.

Fabrication (Execute Gerber Template)

Opens window Gerber Output that allows generating a file in Gerber ASCII format containing NC-Drill Template. Select this option and click on execute button to generate the Gerber file for the template. The report file is displayed immediately. The apertures used for the drill template are listed under the Apertures tab.

Export in GenCAM Format

Allows to export the selected project contents to GenCAM format. This is a special format generated which is accepted by photoplotter other than Gerber.

GERBER Output - An Introduction

GERBER is the standard format used as input to photoplotters that generate the design data on films. These films are used as masters for manufacturing the PCB, the physical realization of the schematic data. GERBER format is a vector format for defining various elements of the layout. This format represents all traces as draw and the pads that are part of the component footprint as flashes. The Photoplotter uses this command language.

The steps for generating a GERBER output is as shown in Fig.10.6:

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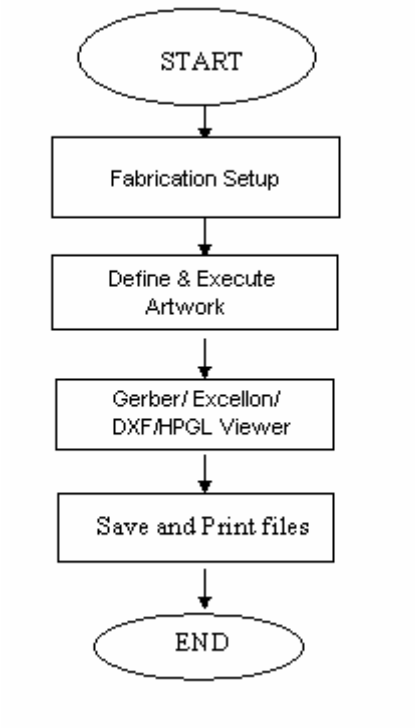
The layout design has to be defined as an Artwork file to view the GERBER output format. GERBER output parameters such as Aperture sizes, no. of copies etc. may then be generated from GERBER setup window. The layers to be processed may be selected from the tool **Artwork**  . Here the various options such as Mirror image, Via pads etc. may be toggled Yes/No except for the Copper pour area, which is toggled YES only if a Copper pour area is created on the board. On clicking this option, a window pops up showing the net name and an option to toggle generation of Hrf and SMD pads. Once the Gerber file is generated, its corresponding artwork can be viewed from **Gerber / Excellon / DXF / HPGL Viewer**



GERBER Output Parameters

Select Fabrication | Setup menu from the Main menu. A window opens from which select the first node select GERBER Photoplotter data and set the necessary data that is required for the photoplotter. Settings include target directory on the disk where the generated outputs such as output units, GERBER format, zero omission, step repeat, scale factor, offset, space between artworks if film is panelized etc are to be stored.

- **Output file location**

Set the required path where the files are to be generated.

- **GERBER Output format**

The format of the output may be specified here. **RS-274D** GERBER format or extended format **RS-274X** that is, GERBER format with mass parameters with respect to a super set of EIA standards. RS-274X format provides enhancements that handle polygon fill codes, positive/ negative image composting and custom apertures and other features. RS-274X is the default GERBER format.

- **Photoplotter options**

Photoplotter options such as **Interpolation** (used to create arcs for the photoplotter), **Filled Polygons Supported** and **Square Flash** fill for rectangles for providing information for the photoplotter. Embed Offset & Stepping commands and Mixed Polarity plot is applicable only to RS-274X format. All the above-mentioned options are essentially photoplotter information and cannot be viewed by the user.

Two types of Interpolation may be used when generating GERBER files - **Linear interpolation** and **Circular Interpolation**.

Linear Interpolation	This plots a straight line from the present position to the X, Y coordinate specified by the data block. Here, steps in degrees are specified into which the arc is broken as individual segments while creating the GERBER output. This is always used while generating GERBER output for lines.
Circular interpolation	Instead of line segments and arcs, a quarter of a circle will be plotted at a time. This eventually reduces the GERBER size. Even if circular interpolation is enabled, the photoplotter interprets arc stepping wherever required.

- **Aperture table**

If RS-274D is selected, then user may choose the aperture table. If it's RS-274X, the aperture will be embedded by default.

- **Offset and stepping definition**

The factors such as offset distance and stepping may be set here.
The required film size is calculated based on the board size multiplied by number of columns and rows plus offsets and spacing between artworks.

Define Layers and Generate GERBER Output

☛ How to define layers?

Layers are to be defined first in order to generate the GERBER outputs. Select GERBER Artworks node from the Fabrication setup window. You will find a spreadsheet as shown in Fig.10.6.

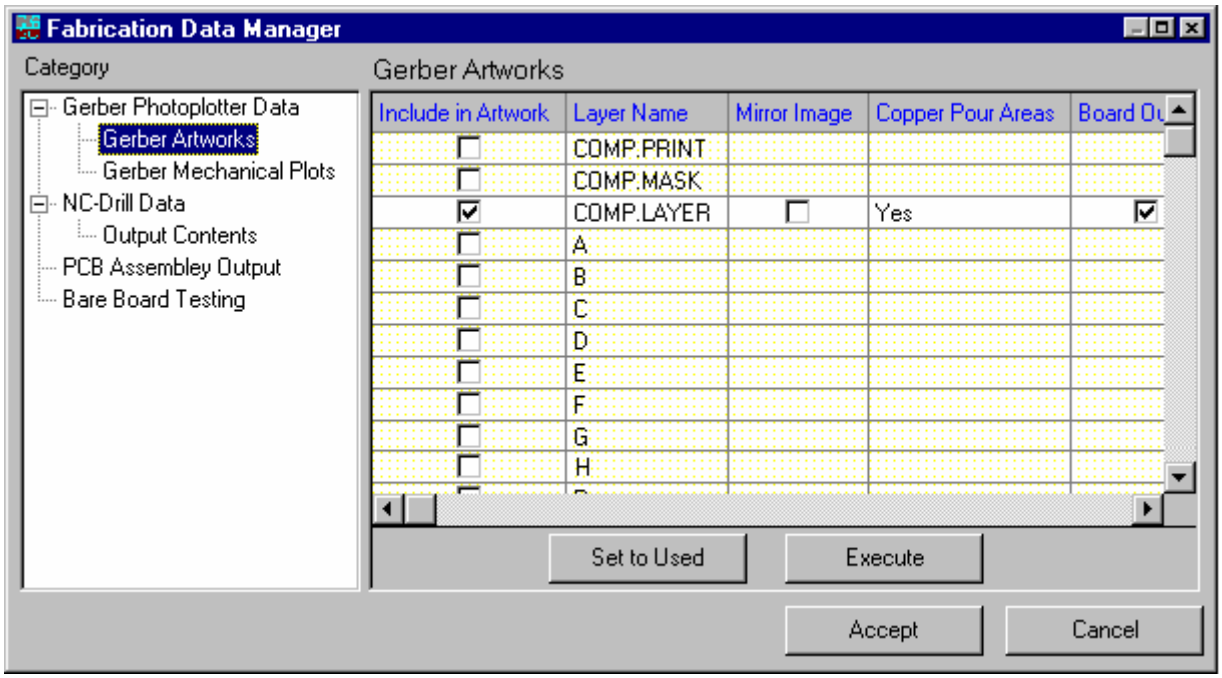


Fig.10.6

Layer defining must be done after setting the parameters in the GERBER photoplotter setup window.

Each layer selected from the list is added to the spreadsheet.

The option Copper Pour Area is automatically toggled from No to Yes only if Copper pour area has been created on the board. Refer to Fabrication Tasks in Fabrication help regarding Optional creation of Copper planes and Copper Pour areas.

Click **EXECUTE** button provided in the window or follow the steps below.

How to generate GERBER ASCII files?

Click **EXECUTE** button in the GERBER Output dialog to display the aperture table required for the selected layers.
Here two files will be generated. One is report file, which contains all necessary information for the photoplotter house to properly process user GERBER files. Report file is automatically displayed after finished output. This feature cannot be switched OFF. The other is the *.ALS file which contains list of Apertures used and is optional. Click close to exit. The generated Gerber files maybe viewed/edited with any CAM/Gerber CAM software.

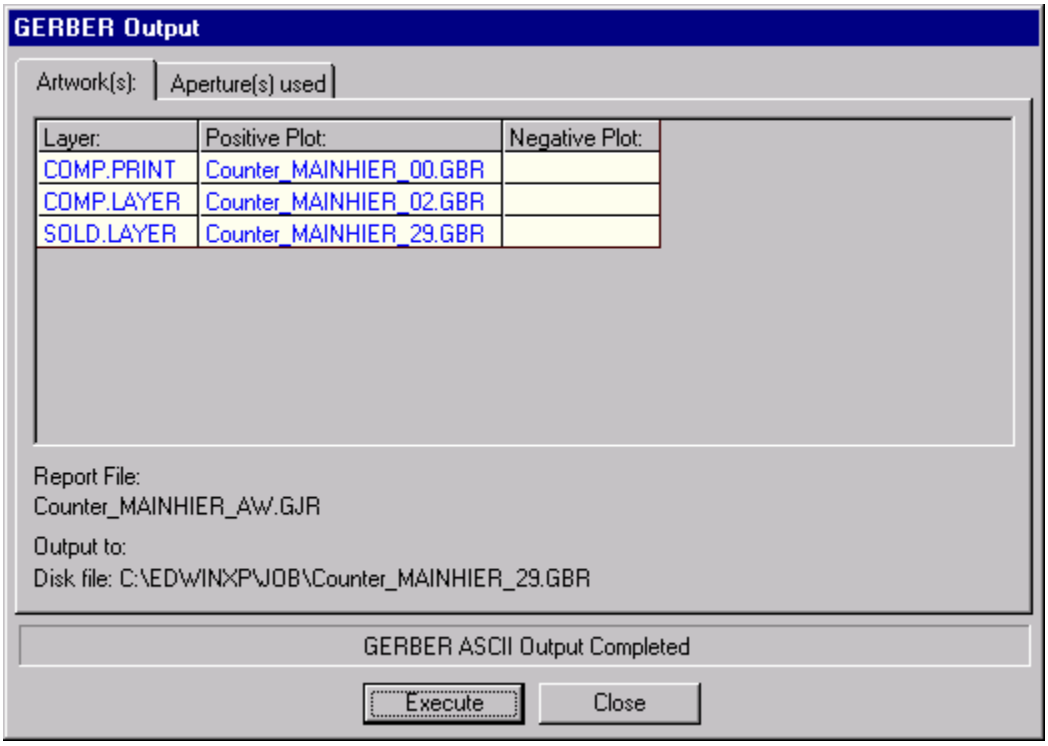


Fig.10.7

Generated files are saved on disk. The file names use the first six letters from the database name. For e.g., if the database is COUNTER.EPB, then the generated files will be as follows **COUNTE00.GBR**, **COUNTE02.GBR**, **and COUNTE29.GBR**. The

numbers correspond to the layer numbers starts from **COMP.PRINT** as 00 and **SOLD.PRINT** as 31. If the artwork contains Copper pour areas then, files with name suffixes 50+ Layer number (negative) will be generated which acts as the main file (applicable only if the Gerber files are of RS274D format).

This completes the generation of the **GERBER** data.

Preview the GERBER Data

How to preview the GERBER data

To preview the GERBER data Select File / Gerber/ Excellon/ DXF/HPGL Viewer and open the .gbr files to be viewed. Different modes of settings may be done using this viewer.

You will observe the selected layer in the display area. For e.g. in figure, GERBER file generated for COMP.LAYER (with Copper Pour Area) of a project is shown in Fig.10.8.

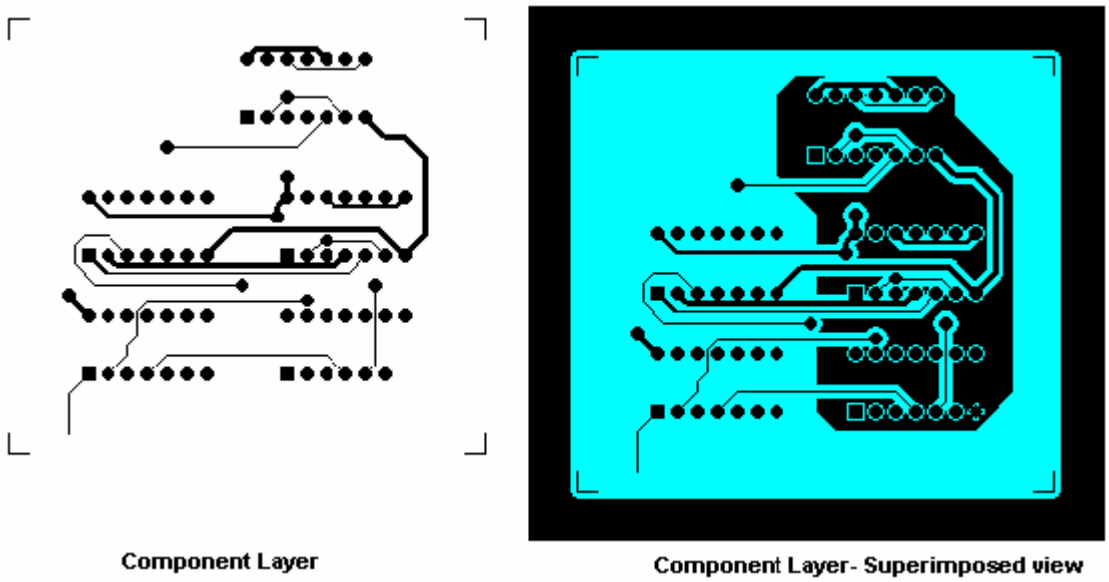


Fig.10.8

The above procedure must be repeated for all the required layers. Note that once artwork files are created it is possible to switch between preview of different layers by direct selection of one of these files.

Add Notes to GBR Files

Notes may also be generated and viewed in GERBER files generated. These notes form the mechanical details of the PCB layout. The plot may include board outline, dimensions, board description notes, holes and pad.

Select GERBER mechanical plot from Fabrication setup dialog box and set the necessary options.

*Only on COMP.PRINT and SOLD.PRINT, the mechanical details may be generated. The storing files are**90.GBR for COMP.PRINT and **91.GBR for SOLD.PRINT.*

To display Notes, check Board description notes. When Pad frames option is checked, the layer may also be set. This enables the pad frames of the selected layer on the COMP.PRINT OR SOLD.PRINT. After defining the required settings, click EXECUTE to execute the plot.

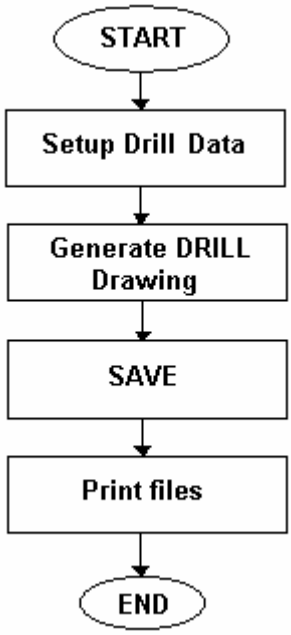
Once again click ***EXECUTE*** to list the apertures required. By default the created GERBER file has .GBR extension with the first six letters of the file name being the first six letters of the project name and the last two being 90 for component side and 91 for solder side. Here two files will be generated. One is report file, which contains all necessary information for the photoplotter house to properly process user GERBER files. Report file is automatically displayed after finished output. This feature cannot be switched OFF. The other is the *.ALS file which contains list of Apertures

used and is optional. For these files the first six letters of the file name correspond to the first six letters of the Project name and the last two will be MK to indicate that it is a mechanical plot file.

Refer Preview the GERBER data in this chapter to preview the resulting plot file.

Introduction to NC Drill

In generating the NC-Drill, the system extracts information about the whole positions, sorts them according to drill size information. The different hole sizes are grouped together and generally sorted to drill in a specific order. This grouping may be done based on sizes, type of drilled hole, like through plated or non-plated, via type like buried or unburied etc. This is generated as a drill tape data. The data may be used directly on any numerically controlled drilling machine. This NC-Drill data is of the EXCELLON format which is the accepted industry standard.



The steps for generating a NC-Drill output is shown in Fig.10.9:

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Before defining NC-Drill data, it is necessary to set up various parameters. These parameters are briefed in NC-Drill Input parameters.

NC Drill Output Parameters

Select NC-Drill Data from Fabrication data manager dialog box. Depending on the equipment used by the PCB manufacturer some parameters must be set prior to generation of NC drill files.

Parameters include:

Output units: inches or millimeters.

Holes to be included on drill data, component pins and vias are default

Omitted Zeroes: Leading or Trailing. By default it is trailing

Optimization method.

A precision format of 2.4 for inches and for 3.3 for metric is selected internally by the program.

Generate NC-Drill Data

How to generate NC-Drill data?

After setting the parameters under the output contents, start execution of this routine by clicking on **Execute**. This opens an NC-Drill Output window as shown in Fig.10.10.

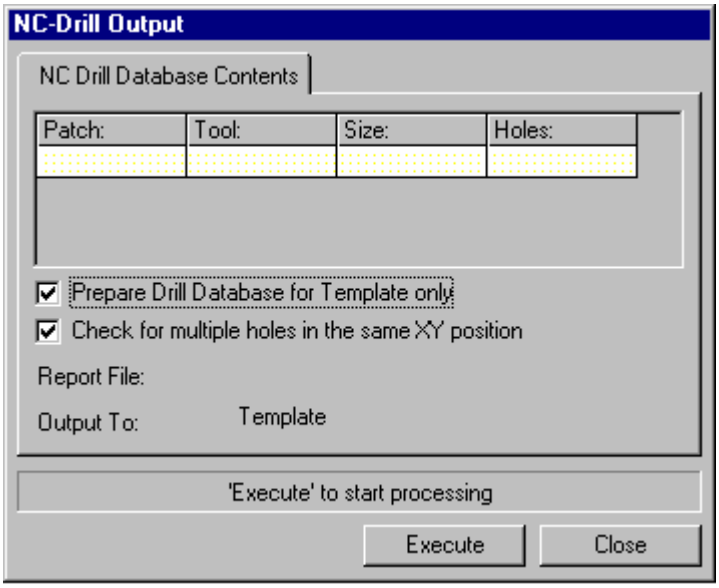


Fig.10.10

There is an option to generate only the template without generating the drill database and also to check for multiple holes at same location. This may be done by enabling the corresponding check boxes. To output the drill data to template check Prepare Drill Database for template only and click EXECUTE to implement the operation. An additional Report file will be created when the output is taken to the Disk file. This file (*.DJR) should be sent to the manufacturer along with the NC Drill database file. To output the drill data to the disk file (i.e., without selecting the check box Prepare Drill Database for template only), click EXECUTE to pop up a "Select/Define NC Drill File Name" where the path and name of the NC Drill file may be defined to execute the drill generation. By default, the created GERBER file has *.NCD extension with the first six letters of the file name corresponding to the first six letters of the database name and the last two letters corresponding to the layer number in the case of through holes. In the case of buried vias, the file extension is Nxx where "xx" corresponds to the sandwich number. The user is allowed to change only the first six letters of the file name. The text box displays the progress of drill generation. The tool data and the number of holes drilled are also displayed.

Add Dimensions/Notes to Drill Template

☛How to add dimensions to drill template?

Textual and graphic details as well as dimensions may be added to drill template drawing before printout.

To display and add dimensions to drill template select Tools/Template (dimensioning) from the menu bar.

Linear dimensions are generated between positions of two contact points.

Select the  **Set Contact Points** tool. You may set up to three contact points. Use the **F1** key to set the first contact point at say top left corner of the board by positioning the cursor at this point and clicking the left mouse button. Similarly set the second contact point using **F2** at say bottom left corner of the board.

Select  **Place Dimension** tool. You will now see several options to position the dimension between the preset contact points. Since you have chosen the vertical dimension, use **F1** and click anywhere to the left of the board. You will observe dimension lines and arrows. Position them alongside the board at a distance by placing the cursor at that location and click. The text containing calculated distance appears attached to the cursor. Place the text to the required position. Dimension text may be rotated during relocation. You can similarly dimension the horizontal side of the board as shown in Fig.10.11.

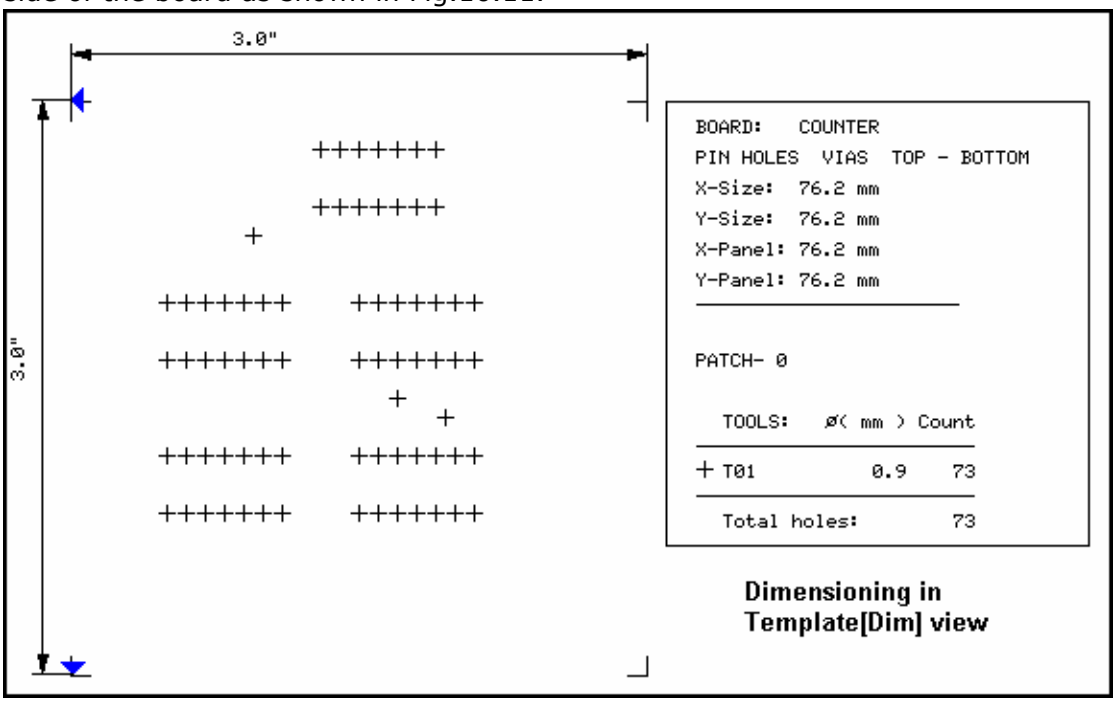


Fig.10.11

☛How to add manufacturing notes to drill template?

Some PCB manufactures require drill template drawing as additional documentation. System creates drill template automatically during NC drill data generation. It contains board outline and symbols for different hole diameters placed at hole coordinates. The legend contains statistics and list of hole diameters with corresponding symbols on the template.

To display and add any necessary manufacturing notes to drill template select Tools/Template (notes) from the menu bar.

The tools are similar to the Design/Page notes in schematic editor.

Introduction to PCB Assembly outputs

When the manufacturing volumes are high and high in component density, designs like SMD, manual assembly becomes difficult. In such cases, automatic component insertion technique is required in a specified format to drive automated machinery to position the components at exact location. As this data is machine specific, there is a provision for both Generic as well as IPC-D-355 standard format of the output.

{bmc get8_10.bmp}

Fig.10.12 shows the steps for generating a Pick & Place output.

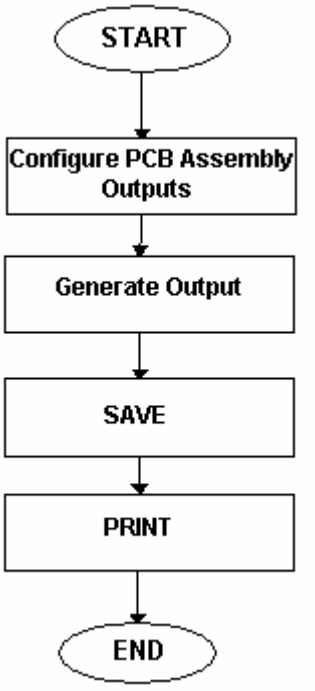


Fig.10.12

☛How to Generate PCB Assembly outputs?

To setup parameters for PCB Assembly outputs choose PCB Assembly output node from Fabrication data manager (Fabrication | Setup).

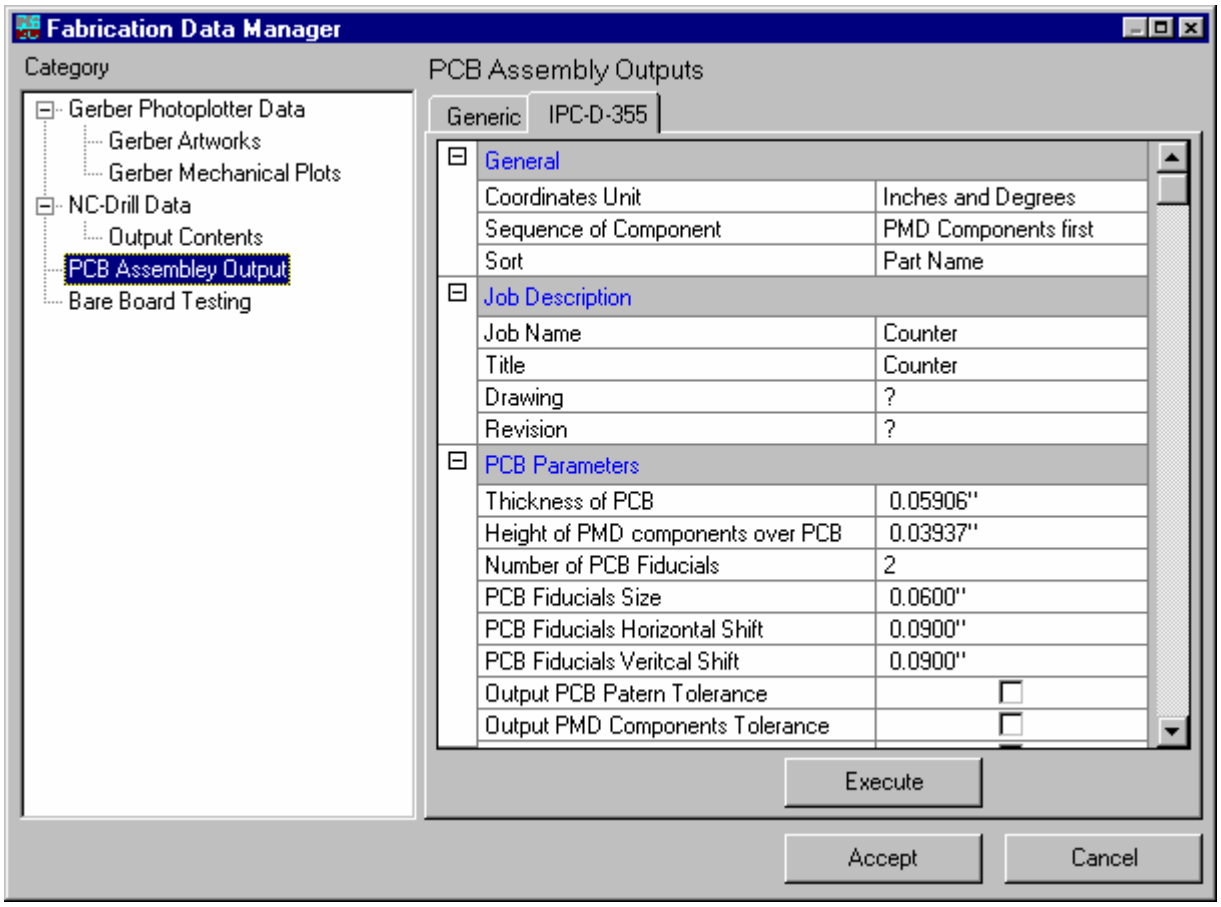


Fig.10.13

Introduction to Bare Board Testing outputs

This is a special on board test outputs generated in Generic and IPC-D-356A standard format.

Fig.10.14 shows the steps for generating a BBT outputs.

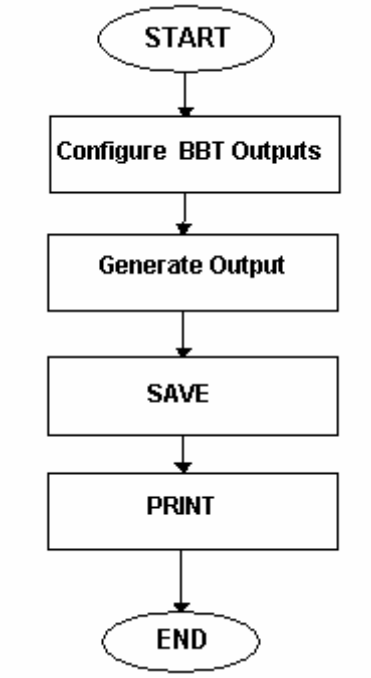


Fig.10.14

☛How to Generate Bare Board Test outputs.

To setup parameters for Bare Board outputs choose Bare Board Testing node from Fabrication data manager (Fabrication | Setup).

Choose either format and set the required parameters. Click EXECUTE to generate the Bare Board Testing output in either Generic or IPC-D-356A format.

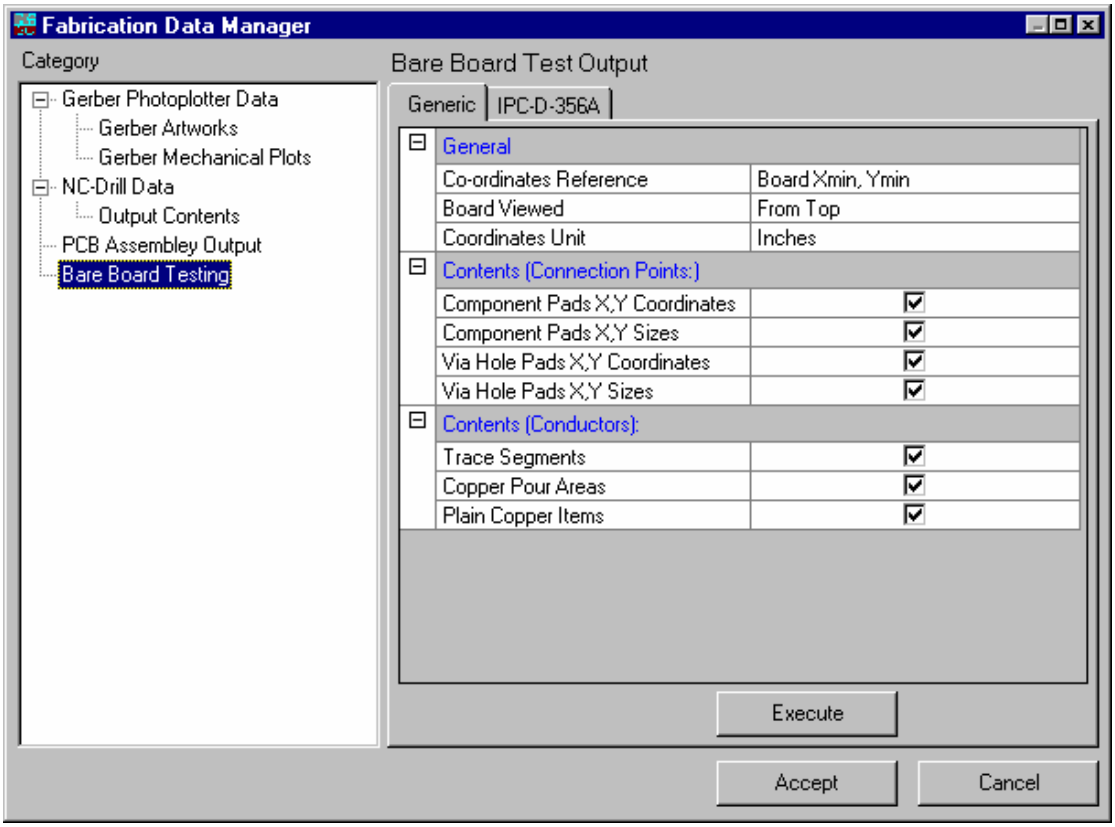


Fig.10.15

Coordinate reference defines the reference point for generating the pick and place data. Normally, it is in the left-hand bottom corner of the board, the board X min, and Y min. alternatively, it could be the origin of the database.

Contents (Connection Points): Defines the reference point for every component that is to be included into the placement information. The available options are:

Component Pads X, Y Coordinates
Component Pads X, Y Sizes
Via Hole Pads X, Y Coordinates
Via Hole Pads X, Y Sizes

Contents (Conductors): Defines whether the placement data must contain trace segments, copper pour areas, and plain copper items.

Click ***EXECUTE*** to generate the pick and place output in either Generic or IPC-D-355.

Graphic Import Editor

Graphic Import Editor makes Reverse engineering possible from GERBER files.

The function of this feature is to import/ reconstruct (reverse engineering process) a PCB from the final outputs generated using any E-CAD/ CAD software (RS 274 format). As of now, *.GBR, *.DXF files can be handled and convert these to

intermediary artwork format (This may be done in Fabrication Manager | File | Gerber/ Excellon/ DXF/HPGL Viewer). Finally, using the Reconstruction tool each object is reconstructed individually in order to reconstruct complete or selected parts of Project Database.

Few examples where graphics imports may be used:

a. Complicated PCB outline with or without cutouts have been drawn using AutoCAD. Resulting graphics can be imported and used to reconstruct same PCB outline in the Project.
b. User has old GERBER ASCII files for a PCB that requires changes in the artwork(s) These files can be imported and updated to obtain new corrected set of artworks.
c. User has old GERBER ASCII files for a PCB but needs matching NC Drill data. These files can be imported. Graphic Import Editor has tools that allow reconstruction of drilling data.
d. Reverse engineering: Old GERBER ASCII files may be imported, edited and used as templates to reconstruct complete Project Database.

GenCAM format

Export in GenCAM format - This is a special format generated, other than Gerber, which is accepted by photoplotter.

Chapter 11

3 - Dimension

Introduction to 3D

Designed electronic circuits (PCB) are usually housed inside cabinets or any intricate structures where spacing between different boards placed has to be dealt with prudently. Working in 3D environment facilitates optical design check. It provides an in-depth analysis of the board density and a realistic view of a designed PCB.

The concept of 3D has been incorporated into **Layout Editor** and **Library Editor** especially for package creation. Layout Editor allows only viewing the board in 3D; no editing can be done on the components or traces. But Library Editor allows editing packages and cabinets. Tools have been provided to view the board and package from various directions and from different angles.

Let us have a look at how 3D has been implemented in Layout & Library Editors.

3D in Layout Editor

Layout Editor is provided with two tools namely 3D Board Viewer and 3D Trace Viewer. These tools may be activated from the menu Tools or from Tools toolbar. 3D View Control dialog contains useful tools to control working in 3D environment. These can also be invoked from Layout Viewer.

3D Board Viewer

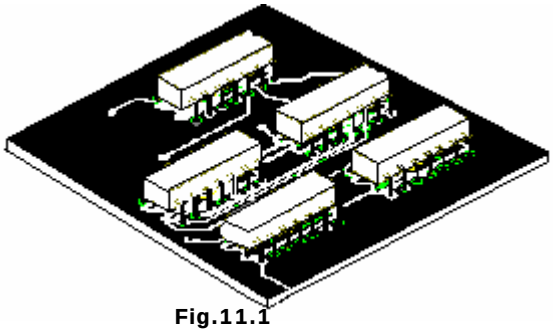


Fig.11.1

3D Board Viewer gives a real life view of the designed board in various perspectives and directions. It gives idea on how the components are located, whether there is risk of friction between components due to their height and shape, the side on which components are placed, etc. This helps to take any design changes if required. Thus it provides a 3D view of the entire board in any of the X, Y or Z planes from different angles. It also provides the facility to view the board from different directions namely north, south, east, west, etc.Fig.11.1 shows 3D view of a finished board inclined at 45º along X - axis and –65º along Y-axis.

When clicked on  3D board Viewer to get a 3D view of the loaded board a 3D View Control dialog pops up, which assists in aligning the board in different angles.

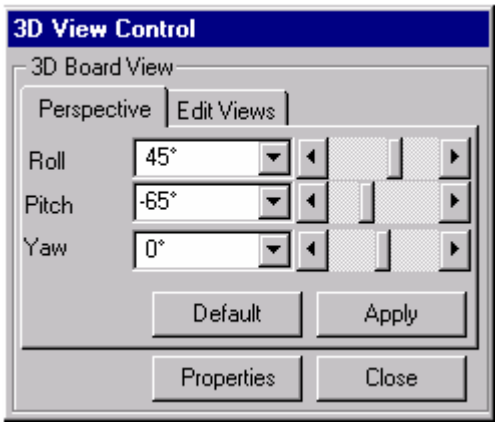


Fig.11.2

Perspective

The controls in this tab allow rotating the board in X, Y and Z planes.

Roll To get an angular rotation of the board along the X plane, select an angle from the drop down list or slide the corresponding scroll bar.

Pitch To get an angular rotation of the board along the Y plane, select an angle from the drop down list or slide the corresponding scroll bar.

Yaw To get an angular rotation of the board along the Z plane, select an angle from the drop down list or slide the corresponding scroll bar.

Click on **APPLY** button to register the values. Click on **DEFAULT** button to get the default values.

3D Edit Views

Click on any option to get a corresponding view of the board from that direction.

Fig.11.3

Properties

Click on **PROPERTIES** button to get a dialog as shown in Fig.11.4.

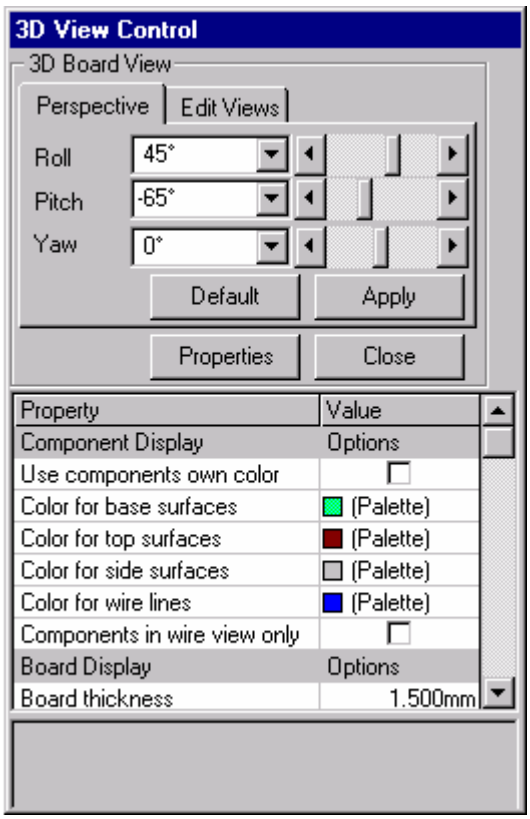


Fig.11.4

Given below is a brief description of each property.

Use components own color Check this column to allow components use its own color.

Color for base surfaces If Use components own color is not checked, select color for the base surface from the palette.

Color for top surfaces If Use components own color is not checked, select color for the top surface from the palette.

Color for side surfaces If Use components own color is not checked, select color for the side surface from the palette.

Color for wire lines Allows selecting color for components outline.

Components in wire view only Check this property to get outline view of components.

Board thickness Allows to specify value for board thickness.

Display top pads Toggles on/off the display of top pads.
Display bottom pads Toggles on/off the display of bottom pads.

Display holes Toggles on/off the display of drilling holes.

Display top side silkscreen Toggles on/off the display of top side silkscreen (component print layer).

Display bottom side silkscreen Toggles on/off the display of bottom side silkscreen (solder print layer).

Display top side traces Toggles on/off the display of top side (component layer) traces.

Display bottom side traces Toggles on/off the display of bottom side (solder layer) traces.

Color for board top side Choose a color for board's top surface from the palette.

Color for board bottom side Choose a color for board's bottom surface from the palette.

Color for board edge Choose a color for board's edge surface from the palette.

Color for board wire lines Choose a color for board's outline from the palette.

Highlight color for surfaces Displays color palette to choose a color for surface of a highlighted component. The component may be highlighted using the tool Redraw | Component in Standard toolbar.

Highlight color for wires Displays color palette to choose a color for outlines of a highlighted component. The component may be highlighted using the tool Redraw | Component in Standard toolbar.

Highlight color for lines Displays color palette to choose a color for print layers of a highlighted component. The component may be highlighted using the tool Redraw | Component in Standard toolbar.

3D Trace Viewer

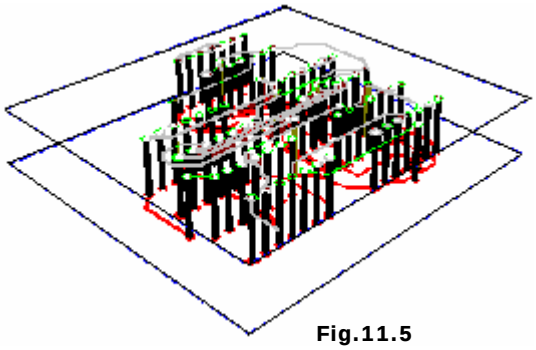


Fig.11.5

3D Trace viewer helps to visualize all the physical connections on board. Traces, vias, buried vias, and copper pour elements can be easily visualized. It helps to examine in detail the path taken by traces of each net .Thus it provides a detailed view of all the traces present on the loaded board by aligning the board in various angles. All the traces placed on the component layer may be viewed from top, while the solder layer traces may be viewed from bottom. Viewing the board from any other direction displays the traces present in other layers. It makes the traces present in internal layers (A to Z) visible as shown in Fig.11.5.

When click  3D Trace Viewer to get a 3D view of the traces present in the loaded circuit. A 3D View Control dialog pops up, which helps in viewing the trace details from different angles.

No operations like loading, relocation, rotation etc can be performed on the components or traces in 3D - view environment of Layout Editor. Only the board as a whole can be aligned in different directions.

Connectivity Test

The purpose and operation of 3D Trace Viewer Connectivity Test is the same as Connectivity test under function tool Nets.

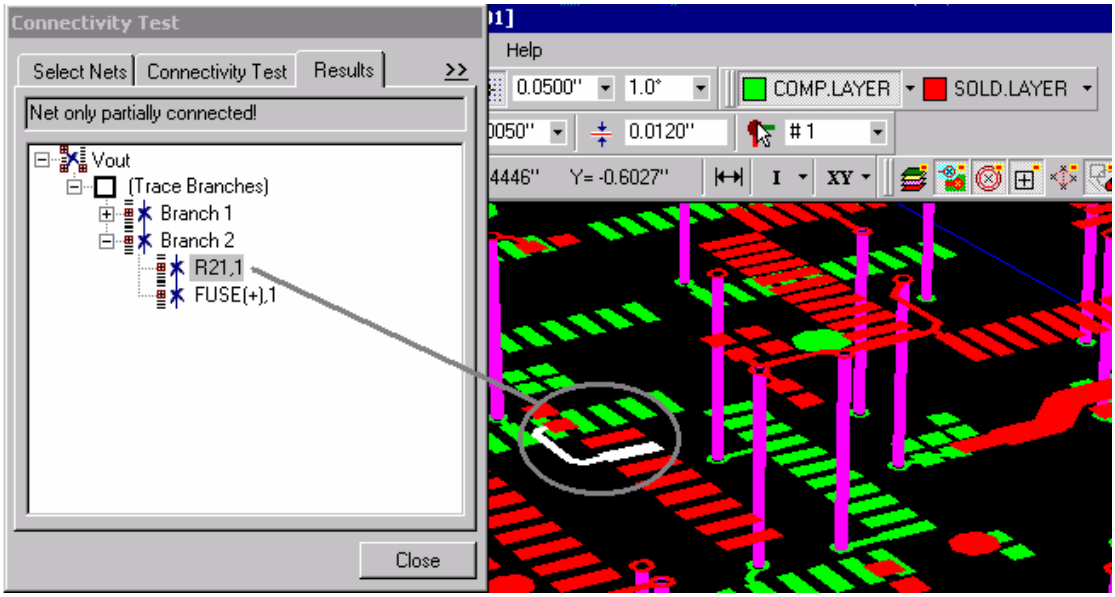


Fig.11.6

However viewing the test results in 3D, gives a deeper insight into the path traversed by the nets thereby helping easy detection and rectification of faulty nets.

3D in Library Editor

In Library Editor, 3D has been bundled with Package Creation. Also a new concept of Board Cabinet has been introduced.

Package Editor

In Package Editor, apart from 3D View Control dialog, a number of function and option tools has been provided to assist the user in editing and orientating the package. A package created in the usual (2D) manner can be converted into 3D using these tools. One can enter the 3D mode from the menu Edit/ 3D Viewer. Package Viewer helps to view the package in 3D.
To begin with, when you open Package Editor in 3D Edit mode, you see a small rectangular box with a round pad on it. This is the same default pad, which appears when a new package is opened in Package Editor. In other words Package Editor gets depicted in 3D mode. Fig.11.7 explains this.

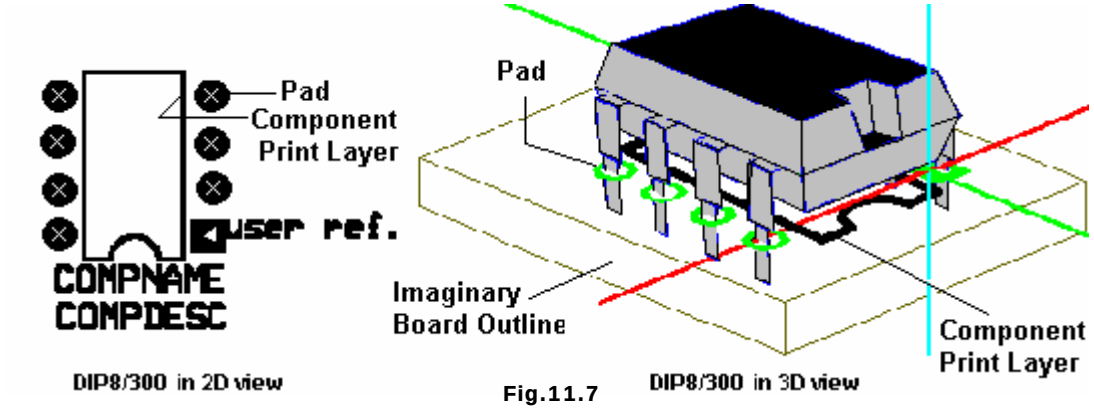


Fig.11.7

Launch 3D Library Editor

The 3D editor can be launched by selecting the menus - Package Editor | Open Package for Editing - (Enter DIP8/300) / Edit menu / 3D Editor.

The 3D workspace is displayed with three perpendicular axes and a default board containing the outline of the DIP8/300 package as shown in Fig. 11.8.

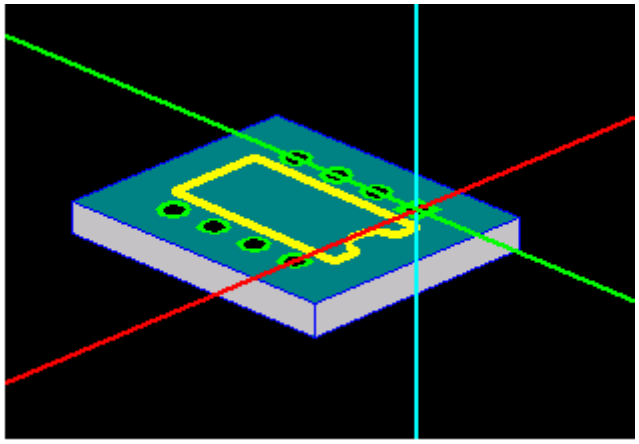


Fig.11.8

The actual view of a DIP8/300 Package is as shown in Fig.11.9.

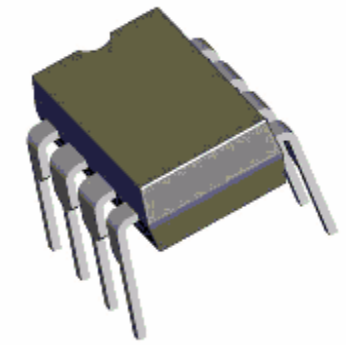


Fig.11.9

A package similar to this figure has to be created using the 3D items. The creation of the 3D package would have been easy if it doesn't have a semicircular notch on the top of the package. There are two ways of doing it. One is to load a rectangular block and then place a semicircular bar at the location of the semicircular notch. However to make the 3D view more sophisticated it is possible to create the package as one composite figure using Polyshape. Since the tutorial aims to acquaint the user with all kinds of 3D items, the main body is created as a collection of basic shapes and the pin is created as a polyshape.

The tutorial illustrates how to create the two fundamental parts of the 3D package

1. The main body – consisting of the rectangular bar and the semicircular notch
2. The pin of the package. Once a pin is created it can be duplicated using Repeat Graphic Item option tool.

Main body

3. Select the Function tool Create 3D Graphic Item -> Select the Option tool Create Rectangular Bar.

4. The option tools With Bottom surface, With Top surface and With Side surface(s) may be enabled to get a solid 3D package.
5. Click anywhere in the workspace, a rectangular bar will be placed with the center of its base placed on the intersection of the 3 axes. The rectangular bar will appear highlighted to indicate that the present focus is on it. Relocation and stretching may be carried out here. By default the Function tool Relocate 3D item gets enabled.

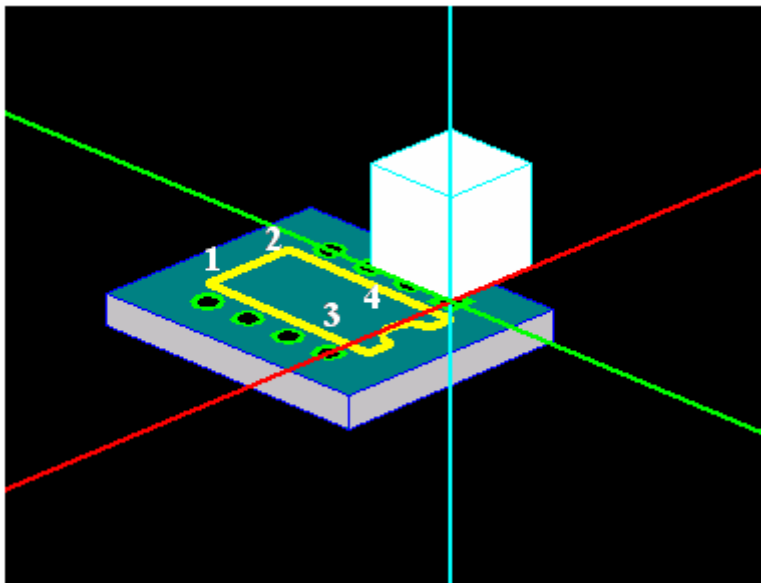


Fig.11.10

The rectangular block has to be relocated and stretched to fit in the area 1-2-3-4 as shown in Fig.11.10. The height of the rectangular bar should be set to the height of the body of the DIP8/300 package (this data is available in the datasheet). The height can be set in two ways.

a. Stretch the item to the required height.
b. Enter the height in the Property window of the Rectangular bar.

6. Relocate the bar. Relocation of the block may be achieved by placing a contact point. A contact point is by default placed on the intersection of the 3 axes. To move the axes to a desired point press SHIFT and click in the direction where it has to be placed.
7. After moving to the desired location press Finish Relocation(F6)
8. Change the height of the rectangular bar according to the value given in the datasheets.
9. Stretch the bar to fit on the component outline
10. Create the circular patch in the package. Load a semi-cylindrical bar.
11. Elevate the body of the package (both the rectangular bar and the semi-cylindrical bar) by around 15/20 mils (.015”) above the board. This can be done by entering this value in the Properties Window (adjust the Z position).

Creation of pins

So far the creation of the package required only the basic geometric 3D items like rectangular bar, semicircular cylinder etc. Operation on these items is such that their basic shape is always preserved.

For e.g. the item given below when stretched will maintain its aspect ratio, i.e. it will have a proportionate increase in volume since it is a basic 3D item.

Consider a 3D item as shown in Fig 11.11

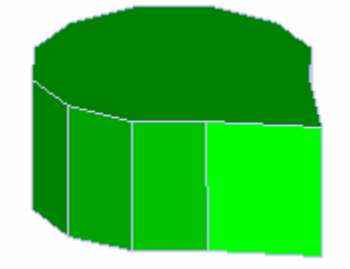


Fig.11.11

This is a composite figure which can be derived from the basic shapes. For e.g.:, a circular cylinder can be loaded on the workspace and it's angular snap if changed to 30 degree (using it's Property window) will turn the circular cylinder to a bar with 12 vertices. Now if one edge of this bar is pulled away from the center the composite shape shown in the figure can be obtained.

In order to cater to situations where such figures are needed, Library Editor defines a general term called POLYSHAPE. A polyshape is a 3D item which has been derived from a basic 3D item and whose edges and vertices can be stretched (unlike those of 3D basic items).

The pins of a DIP package are composite figures. Using 3D Library tools, a pin which is shown in Fig.11.12 can be created.

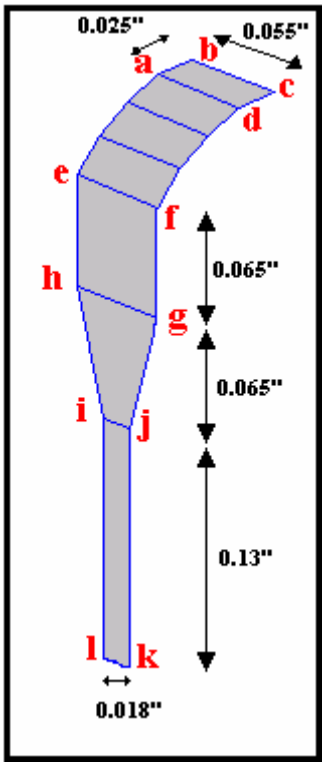


Fig.11.12

This can be derived from a semi-circular strip by stretching its vertices and edges.

12.

1. Load a semi-cylindrical strip on the workspace and move it to a distance away from the other items -> Finish Relocation

2. Set the height of the strip to around 0.055”. This will be length of sides bc / ad etc.
3. Set the number of vertices to 8.
4. Angle B = 90
5. Z Rotation = 90
6. X Rotation = 90

Now the item will look like

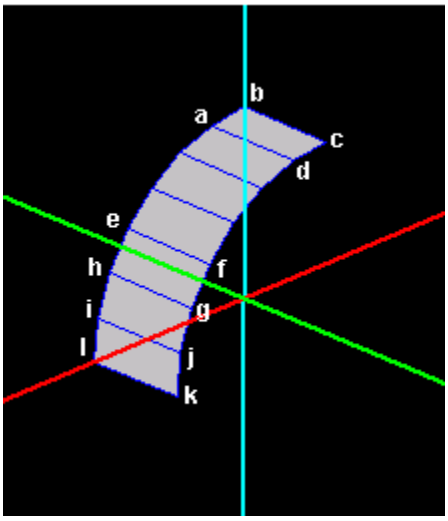


Fig.11.13

13. Once all the settings are made, the semi-cylinder can now be turned into a polyshape so that its edges and vertices can be stretched.

14. Select the Function tool Convert 3D item to Polyshape and click on the semi-cylindrical strip.

15. Creation of face "abcd"

16. Refer the picture of the pin. The length of 'ab' is .025". As a rule of thumb, selection of edges is easier in Perspective View and setting dimensions in 2D views, like From South. Select Stretch item and select the first edge. Now select tab Edit Views in the 3D-view control and select From South. Now move the vertex such that it coincides with the adjacent vertex.

17. After the two coincide, select a Snap value of "ab" i.e. .025", press Shift key and click in the positive x-axis. Press Finish stretch. The face "abcd" of the pin is formed.

18. Creation of face "efgh".

19. Select the edge "gh" in Perspective Default View in 3D View Control and then move to the Edit Views -> From South view. First merge the two edges and then select a snap of .065" (the distance separating the edges ef and gh) and click on the negative z axis to complete creation of the face "efgh".

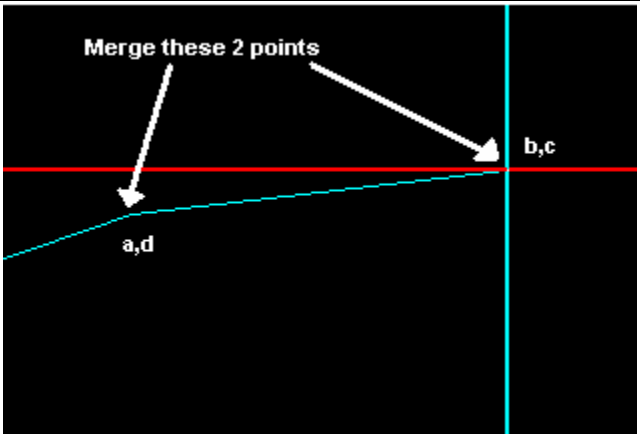


Fig.11.14

20. Creation of face "ghij" and "ijkl" .Select the edge "ij" and merge it with edge "gh" using the same method mentioned in the above steps. Now select a Snap value of 0.065" (distance separating the edges ij and gh) and click in the negative z axis. Repeat the same procedure for the face "ijkl".
21. As shown in the picture, the length of "ij" is lesser than that of the other edges (0.018"). To set this move to the Perspective Default View in 3D View Control and select the vertex i. Now stretch it along the y axis to a desired position. Press Finish Stretch. Repeat the same procedure with the vertices k and l.
22. Now repeat the pins for the rest of the package and place them in the pad holes in the 3D board of the editor to complete the 3D package of DIP8/300.

Board Cabinet

Printed Circuit Boards are usually housed in complex mechanical structures. These structures can hold large number of such boards. In such situations it becomes necessary to evaluate the spacing between boards, proper utilization of available space, etc.

Board Cabinet Editor helps to create cabinets of various shapes and arrange boards within those cabinets. It assists in editing and orientation of all boards present in the project. It also provides 3D view of all the boards placed, thereby giving a real life appearance of the cabinet as a whole.

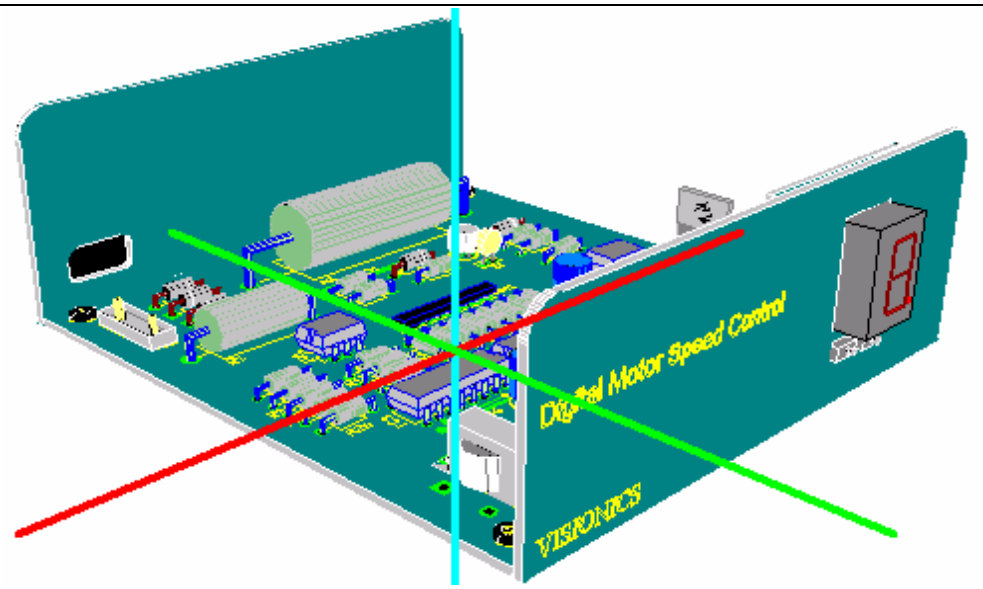


Fig.11.15

Board Cabinet editor window details are mentioned below

Points to remember

Before starting straight away with design in 3D, certain points have to be kept in mind. These include:

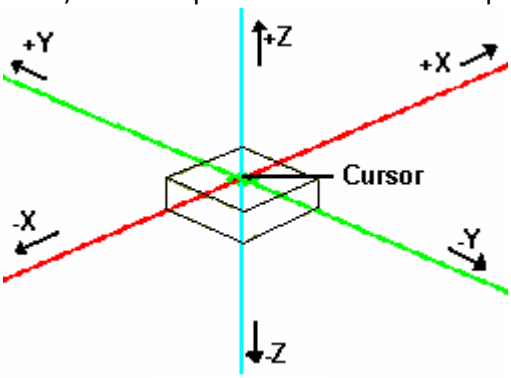


Fig.11.16

- 3D graphic items can be edited only in Library Editor. Layout Editor gives only a real life view of the designed board from various angles and directions.
- You can select pre fabricated 3D elements from 3D elements library while creating 3D packages for components or board cabinets.
- In 2D, mouse cursor can be used to select co-ordinates, by just clicking at that particular point. However in 3D, obtaining the co-ordinates is not as simple as a mouse click since we have to work with co-ordinates placed in 3 planes (X, Y & Z). The three axes act as cursor and to locate a point, each axis has to be moved individually to that point. This is achieved either by clicking on the axes along which the co-ordinates are located or by textually entering the values in 3D View Control dialog.
- The 3D cursor movement can be controlled either from 3D View Control dialog or by using grid/snap values. For quick displacements of the 3D cursor, press ALT key and CLICK at the desired point on the axis along which the

movement has to take place. Using ALT + SHIFT + CLICK moves the cursor to the point and redraws the entire workspace around that point. In addition, the displacement of the cursor and items are also dependent on snap and grid values set. For fine controlled movement, use CTRL + CLICK to get increments with respect to grid value, whereas SHIFT + CLICK gives increments with respect to snap. Precision value determines much finer movements (effective only when snap is OFF). These movements can be easily noticed when working in 3D View Control dialog.

- 3D View Control dialog has all the controls for orientating the board and setting properties of 3D environment. Perspective view helps to select items easily, whereas, Edit Views mode helps in fine editing of the selected item.

- To reduce the time required for redrawing items, enable the display of only the required and most necessary items in the workspace.

- While using 3D cylindrical graphic items, if shape of the item is not of much significance then setting a high value for angular step/ number of vertex in the property dialog, reduces the time required to redraw the items on board.

- Use the property dialog of selected item to carry out swift operations while relocating, stretching, etc.

- Items can be located only at the vertex where the 3 axes meet. Relocation, rotation and stretching of items are all with respect to one of the axis.

Terms to be familiar with:

Polyshape:
Refers to a composite and intricate 3D item derived from any basic 3D graphic item, whose edges and vertices can be stretched.
To obtain a polyshaped item - load any of the basic 3D graphic items, change its angular step using property window (optional), select the function tool Convert 3D item to polyshape & click on the item. The item gets converted and the desired shape can be obtained by stretching the item from its vertices or edges. A 3D graphic item can be converted to polyshape but the reverse is not true.

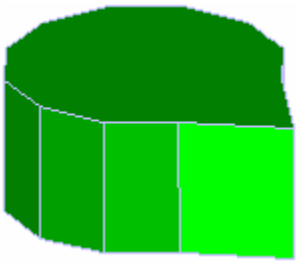
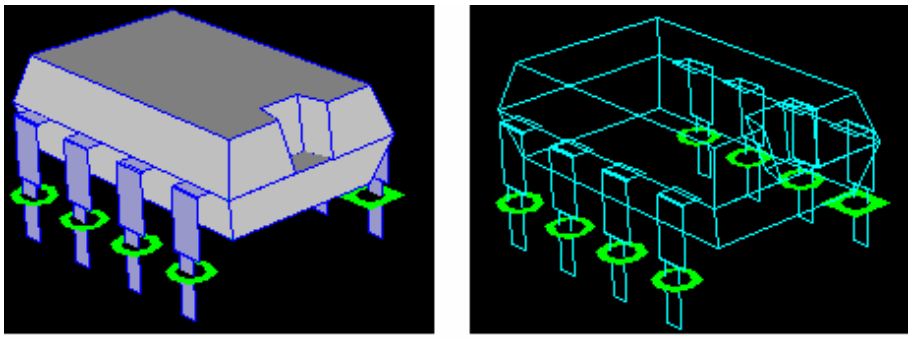


Fig.11.17

Wire view:
Wire view refers to an outlined view of 3D item. Displaying items in wire view reduces the time required for redrawing the item in workspace.



Package with all surfaces Package in wire view

Fig.11.18

Chapter 12

General

Terminology

- Components
  Real life electronic devices present in a project.

- Part
  Virtual representation of a component. Components are loaded into a project as Parts.

- Symbol
  The Schematic or symbolic representation of a Component.

- Package
  Layout or physical representation of a Component.

- Special Parts
  Parts having either a symbol or a package (only), not both.

- Entry Pins
  Schematic representation of points where electrical connections are given or taken.

- Padstack
  An area reserved on the PCB Layout in each layer around the pins for electrical connectivity.

- Vias
  Conductive holes drilled in a PCB for routing through different layers.

- Connections
  Graphical representation of the connections on Schematic Diagram.

- Route
  Physical connections on a PCB Layout.

- Nodes
  The point at which electrical connection exists. Nodes are highlighted in the Schematic as well as PCB Layout.

- Net
  A collection of nodes that are electrically connected together.

Hotkeys, Shortcut Commands and Tool Boxes

Hotkeys

This list is a combination of key press, which allows the user to execute certain operations. The following hot keys are applicable to all editors.

Arrow keys	Moves the cursor in small steps of pixels
Ctrl +F1	Invokes context sensitive help for the currently active topic.
ESC	Cancels the current operation.
Shift	Overrides the snap interval.
Shift +Z	Toggles long/short cursor when interacting with an object (move, route etc.)
Shift +U	Zooms Up at cursor position.
Shift +D	Zooms Down at cursor position.
Shift +B	Zoom Box.
Shift +P	Toggles place reference point at cursor position/ delete reference point.
Shift +G	Toggles snap reference point to closest snap position/delete reference point.
Shift +R	Sets reference point from input box.
Shift +C	Clears all contact points placed.
Shift +S	Copy Box, blocks portion of the work area to be copied to clipboard.
Shift +Q	On-line single trace channel clearance check.
Shift +W	Erases clearance error label texts.
Shift +ENTER	Equivalent to left click (places the object).
Shift +V	Pans the workspace with the cursor position as the new center.
Shift +M	Feature to measure the distance between the selected object (as the reference object) and any other object is included in this version. The distance of measurement is displayed in the status bar provided below the editor. This function is made possible with the help of the Short key command, SHIFT+M. After pressing SHIFT+M

	(message on the status bar prompts to select the object) click on any object. Keeping this object as the centre, move the cursor to any other object on the graphics area. The distance of measurement is displayed in the status bar concurrently, according to the movement of the cursor.
TAB	Each click of the 'Tab' key allows the user to view the previous and present status of the workspace. For e.g., after a Zoom Block operation has been done, click the Tab key. The user sees the workspace before zooming. Another click on Tab key enables to view the current status, i.e., the workspace with the zoomed block.
Page Down/ Page Up	To move between pages within a circuit.
Home	To return to the page/ board datum or the reference point as the center.
Ctrl+Z	Undo the previous operation
Ctrl+Y	Redo previous operation
Ctrl+X **Ctrl+C** **Ctrl+V** **Ctrl+A** **Delete**	Cut Copy Paste Select all Delete selected items.
Backspace	Use 'Backspace' key to perform the function of the first option tool for the currently selected function tool. Usually this hotkey is useful while rotating an object or while retracing a routed connection.
Right click	Simple right click on the workspace displays a floating menu containing the function and their corresponding option tools. Operations may be carried out easily with the help of this menu.

Following are the alternative methods to existing hotkeys.

Zooming

+	Zooms Up at cursor position.
-	Zooms Down at cursor position.

Panning

SPACEBAR, MOUSE MIDDLE BUTTON, SHIFT + Right click, Shift + V Pans the workspace with the cursor position as the new center, so position the cursor first.

Selecting objects

Shift+Click	Starts block selecting the objects enclosed. A bullet marks the selection. On right click, basic edit operations can be carried out in the objects enclosed by the block.
Ctrl+Click	Selection of object(s) is indicated by bullet. The object may then be stretched, moved etc. Also right clicking a bulleted object displays a floating menu containing the basic Edit operations.

To End an operation

END	Ends an operation (equivalent to using the option tool F4 while routing, F2 while adding nodes to a net etc).

Redraw

Ctrl+Home	To zoom to fit the sheet (alternative method for Redraw on Page).
Ctrl+F	To find objects on the page. The *Info* window opens, double click on name in left pane, system redraws positioning the object at center.
Alt+W **Ctrl+SPACEBAR**	To redraw to the current mode selected.

Shortcut commands

This is a combination of key press, which allows the user to directly invoke any object oriented function. This is especially useful when switching between different groups of object oriented functions bypassing selection through menus. A shortcut key operation may be initiated with a * character followed by the key combination. Shortcut keys invoke functions, only in the current editors (Schematic Editor, Layout Editor etc.). E.g. ***CC** invokes the function tool *Open Library* in Schematic Editor if this editor is opened.

Toolbars

Most of the menu items present under each menu have been customized and grouped under different toolbars enabling access in the following two ways:-

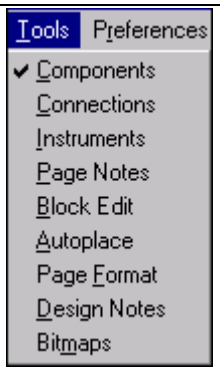


Fig 12.1

1.Enabling the menu item from the respective **menu**
E.g.: Page Format may be selected from under Schematic Editor | *Tools* menu as shown in Fig.1.6.

2. Clicking the tool from the respective **toolbar**.

E.g.: Select  from **Tools** toolbar as shown

Fig. 12.2

Also note that in Fig.1.7, the text displayed by the side of the mouse pointer highlights the function of the selected tool. This text is called *ToolTip* text and is displayed when the mouse pointer is moved over a tool. Viewing of ToolTip text may be enabled/ disabled by clicking on  ***Tooltip*** tool from *View* toolbar. The various toolbars may be made visible/ invisible from the menu *View* | *Toolbar.*

 *A detailed description of the tools selected is displayed in the status bar.*

Standard Toolbar

Displays the tools that controls the working environment of the workspace and is common to all editors. The display of the standard toolbar may be toggled on/ off by selecting its option from View | Toolbars | Standard. The standard toolbar is as shown below.

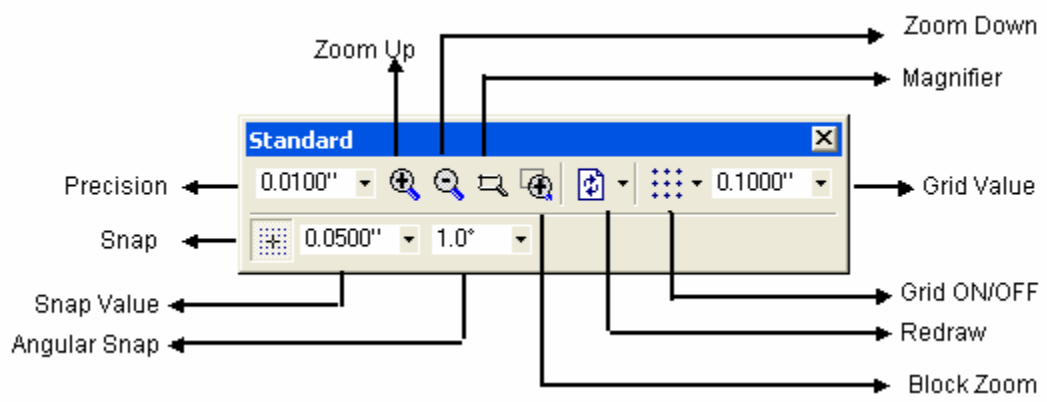


Fig :12.3

Custom Toolbar

Commonly used function tools from different toolbars are grouped in a special toolbar called *Custom toolbar*. A special setup routine (accessed from *Preference* menu) enables to customize Layout of the toolboxes for Schematic and Layout Editor modules according to user's requirements. Typical example is shown in Fig. 1.8.

Practically there is no restriction in placing number of tools in custom toolbar. The toolboxes may be opened for use from corresponding editors and may be placed anywhere on the screen.

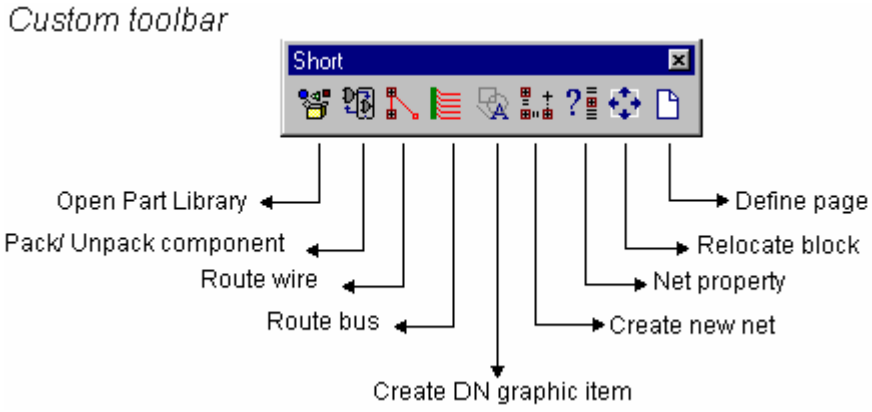


Fig:12.4

How to display / hide toolbar?

It is possible to hide the toolbar, then display it again when required. For this switch ON/ OFF the required toolbar from *View* | *Toolbar* menu in any editor.

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