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BoardWalker9627

Key Features:

- In-Circuit Functional Test Library (Digital/ Analog/ Mixed Signal) of >35K devices
- QSMVI Signature method for testing ASICs / Hybrids &Discrete
- Test logic families : TTL / CMOS / ECL / EIA / LSI / Linear / Memory & more
- In-Circuit IC identify feature for house coded ICs and Ics with their number erased
- Automatic internal pull – up/pull – down for open collector & open emitter devices
- Functional testing can be done without need for learning from known good board or circuit diagram, using Digital Simulators and Analog evaluation software.
- On-line simulation make accurate testing of sequential devices possible even when their Reset pins are disabled in In-Circuit conditions.
- Unique "Best-Fit-Curve" algorithm enhances the fault coverage.
- Board Learn / Compare mode increases board recovery rate.
- Built-in Resistance, Capacitance & Voltage measurement capability.
- Powerful logic waveform display window for failure confirmation.
- Circuit Tracer for schematic generation / reverse engineering applications (Optional)
- IDTE Software for easy Device Test Program Generation (Optional)
- Russian Device Library (Optional)

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BoardWalker 9627 is designed as a affordable Digital, Analog & Mixed Signal Functional test System, to carter the needs of PCB test and repairs depots, keeping in mind the changing PCB Technology & the challenges in testing them. It can effectively test Digital, Analog and Mixed technology IC's in In-Circuit, as wired condition and gives clear PASS-FAIL results. Hybrids, ASICs and house-coded ICs can be checked using QSM signature method.

It is a combinational mixed signal test system with the addition of Integrated Boundary Scan test for the latest generation chips. It also Incorporates an advanced QSM VI with auto "Best Fit Curve" algorithm to enhance the fault coverage. Optional IDTE Software makes new device test program generation easy with graphical user interface.

CAPABILITIES OF BOARDWALKER WITH TESTDIRECTORS SOFTWARE

IN-CIRCUIT FUNCTIIONAL TEST

- Functional Test facility for testing individual ICs in In-Circuit or Out-of-circuit.
- Pin status Check & In-built DRC (Design Rule Checker).
- IEEE Standard VHDL Language in behavioral description of the function of the chip in its library.
- Device programming for SSI/MSI in Qmax Device Description language (QDDL).
- PythonTD Test language for Analog / Mixed signal device stimulus and output evaluation
- Auto compensation is extended for all digitals devices (not limiting to SSI / MSI) and thus LSI / VLSI chips can be tested in its In-circuit configuration without the need to learn from a known good board.
- Unified Library off 33K+ devices & devices test comprehensive report for validation of Library test Program developed by a user.
- Identify "Unknown" devices using advanced foot print match algorithm & covers SSI/MSILSI devices.

USER DEFINED QSM VI STIMULUS

- Standard and user defined wave pattern as stimulus for VI Trace and thus not limiting the VI trace to simple sine wave alone.
- User defined wave pattern can be any mathematical wave shape such as sine/triangle/square/step ramp or even arbitrary patterns as desired by user & can be stored in the library for possible re-use.
- The frequency is fully programmable up to as fast as 100KHz as a result of BoardWalker's vast time base selection capability.
- "Best Fir Curve" –an unique feature, where the best drive pattern is automatically suggested to the user for the characteristics of the UUT to increase the fault coverage.
- Advanced algorithm suggests the failing pin within a device with % probability.
- Use of Step wave is useful in analyzing transient response of node.

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- Frequency sweep generation to trace the frequency response of node.
- Incorporates interactive mode as well as learn & compare.
- Fixed Reference, any pin to any pin or user combination
- Learn net-list from the clip status link option.

MEASUREMENT FUNCTIONS & OTHER UTILITIES

- Resistance / Inductance / Capacitance / Voltage Measurements.
- Diode Measurements
- Frequency Measurements.
- 3 Channel – Digital Oscilloscope with Programmable Load.
- 3 Channel Function-Generator.

TEST SEQUENCER

- For Sequencing of multiple tests with conditional branching, messaging, user promoting, external trigger & external handshake.
- Board level test using combinational of isolated device test (ICFT), QSM VI, Measurements, Card Edge Functional Test, Integrated card edge + boundary scan Test* all in one test program.
- Full graphical TPS development using JPEG image of the PCB under test, tagging device & Pin.
- Adding tests to the devices cluster with just a right click of the mouse learn, verify and test options using mouse click on the device location.

CARD EDGE FUNCTIONAL TEST

- User can develop test program for complex boards with ASICs and BGAs, where no functional data are available.
- User can generate the test vectors using the graphical waveform editor or Phyton TD test vector generator, where the primary I/O pins can be either physical edge pin / In-Circuit pin or JTAG virtual boundary scan pin.
- User can either learn the expected output for a known good board or define the expected output using graphical waveform editor or simulate the expected output using VHDL simulation or the phyton TD test language with mask / tolerance editing facilities.
- Automatic guided probe back tracking for fault isolation upto node level.
- Graphical waveform editor and Phyton TD supports Digital / Analog and mixed signal I/Os.
- The test program developed can be use for a device / cluster or a complete PCB.

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- In case of cluster or whole board, user needs to be inpit the netlist of the circuit, assign input / output pins for tester channel for automatic generation of guided probe back tracking of internal nodes.

BOUNDARY SCAN TEST

- The system meets IEEE 1149.1 standards
- Boundary scan uses simple 5-wire connector (JTGA) to interface to the PCB under test, Eliminating the need for test pin contact (Virtual Test Pin Test Concept).
- Using Boundary Scan Software package and vendor supplied BSD Files, ID Code Read, User Code Read, Integrity test and can be performed.
- Learn and compare option for interconnect test, where no netlist is available.
- Functional Test for BS devices and Non-Boundary scan devices.
- Integrated Card Edge and Boundary Scan Test for Interconnect Test and Board Functional Test.

TESTSTATION

- Programs developed in TestDirector6 TestSequencer can be exported to Test-station.
- Test only function and no program /data /tolerance can be modified.
- Auto run mode / manual run mode with options for stop on first failure, details on failure and graphical mode of testing.
- User defined Error Log Reporting, failure analysis, statistics and data log.
- Optional Remote Monitoring of yield and statistics.

BOARD LEVEL SIMULATION & FAULT COVERAGE (optional)

- Off-line Simulation helps develop TPS without tying up the ATE system.
- Advanced On-line Simulation support for increased fault coverage for boards that fail to initialize
- Fault Simulation software for Board Test Program validation and test comprehensiveness.
- Fault coverage report.

INTEGRATED DEVICE TEST ENVIORNMENT – IDTE (Optional)

- For developing new Digital Device Model in the library using VHDL/QDDL language behavior.
- For developing new Analog/Mixed/signal device models using python TD Test language and adding it in the library.
- Graphical Test Program generation feature.

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CIRCUITTRACER (optional)

- Using multiple clips, edge connector's probes and JTAG I/O pins, the connectivity between devices can be learnt and a netlist created.
- Created net list can be imported into optional Edwin CAD package for schematic generation.

SPECIFICATIONS

MAIN SEQUENCER / CONTROLLER:

- System based on highly programmable dedicated test vector processor
- USB 2.0 Interface between the main sequencer and user PC.
- The system has 1K X 60 Bit RAM for instruction register.
- Basic timing unit programmable from 10ns to 655us in steps of 10ns
- Time duration is programmable up to 256.
- Test vector depth up to 64K.

DIGITAL MODULE (Programmable Palette):

- Minimum of 32 channels expandable up to 64.
- Digital drive speed up to MHz.
- Data rate programmable from 40ns to 160ms insteps of 10ns.
- Drive level up to +12V / -12V programmable , 40mV steps.
- Sense level up to +12V / -12V programmable , 40mV steps
- Memory behind each pin 64 X 4 Kbits.
- High Current Pin driver and the current range is +/-650mA functional and In-circuit operations.
- Pin driver is capable of driving all three states of Hi, Low & Tri State.
- Flying channels upto 4 Nos for guarding purpose.

DIGITAL MODULE (Fixed TTL Palette) (Optional)

- No. of Channels per Card 64 fixed not expandable
- Digital drive speed up to 10MHz
- Data rate Programmable from 40ns to 160ms in steps of 10ns.
- Fixed Drive level of 0V-5V.
- Fixed Sense level of 0.8V-2V
- Memory behind each pin 64 X 4K bits.
- Pin-driver is capable of driving all three states of high, low & Tri state.

ANALOG MODULE

Analog module can be used for mixed signal and analog test. Three independent analog channels can be multiplexed to any of the 64 test channels +4 flying channels.

- Maximum of 3 channels
- Analog sampling rate is 25MS/sec
- Memory behind each pin 64 K X 24 (Drive & Receive)
- Module has 4 different programmable voltage ranges as +/-1V, +/-3V, +/-6V, +/-13V
- Dynamic drive / Receive current maximum up to +/-130 mA / per channels at maximum voltage range.
- Drive pattern Sine/Triangle/Rectangle/Ramp/DC & User definable.
- Multiple user programmable source impedance ranges.
- 12bit resolution of DAC / ADC to provide very accurate results.

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BOUNDARY SCAN (Test Technique Module)

Built in integrated JTAG port on the front panel of equipment along with Digital channels for Boundary Scan Testing and coverage of Non Boundary Scan Devices through Virtual test Pins (BS Pins) and ATE Digital channels.

- Single JTAG Chain.
- Compatible with IEEE 1149.1 standards
- Nominal JTAG Clock frequency is 1 MHz and it can be programmable up to maximum of 10MHz

UUT POWER SUPPLY

- Fixed SMPS power supplies are integrated for UUT testing.
- System has 5 fixed Volt in volt / current ranges of +3.3V@8A, +5V@8A, -5V@8A, +12V@6A, -12V@6A.

GENERAL TERM SPECIFICATIONS:

- Controller: Minimum –Core-i3, 4GB RAM, 500GB HDD, 4-USB slots, keyboard, Mouse, Monitor.
- System should be compatible with windows 7 or later OS based.
- System Power: single AC 110V – 60Hz / 230V – 50Hz
- Operating Temp.: 35C +/-3C
- Dimensions: 4U Cabinet 470(W)X385(D)X230(H)
- Weight: Aprrox. 12 Kgs.

TEST INERFACE

In-Circuit Walking Clips

DIP Clips – Top access& Bottom Access
PLCC Clips
SOIC Clips
TO5 Package
TO9 Package
Russian Device Clips
JTAG – 5 wire simple connector for boundary Scan Test

Out-Circuit

DIP 40 & 64
SMD – SOP/TSOP/PQFP/SOIC/SOJ/PLCC

Customized

Card Edge / Bed of Nails/Automated XYZ Prober (Optional)

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